Low power single channel OP-Amp

Features

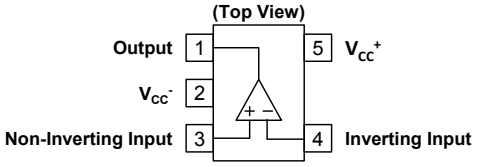
- Input offset voltage : 2.5mV max.
- Input offset voltage drift : 5μV/°C typ.
- Supply current : 0.45mA typ. at Vcc^+=5V
- Input bias current : 20nA typ.
- Input common-mode voltage range includes ground
- Internal ESD protection :
  Human body model (HBM)±2000V typ.
- Integrated EMI filter : EMIRR=84dB typ. @ f=1.8GHz
- Wide single supply voltage range or dual supplies
  +3V to +32V or ±1.5V to ±16V

NJM320AF, NJM321AF
(SOT-23-5)

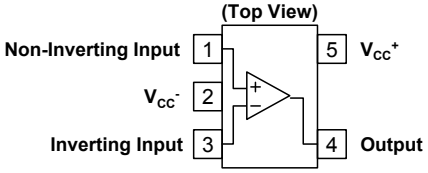
NJM320AF3, NJM321AF3
(SC88A)

NJM321AKG1
(DFN6-G1 (ESON6-G1))

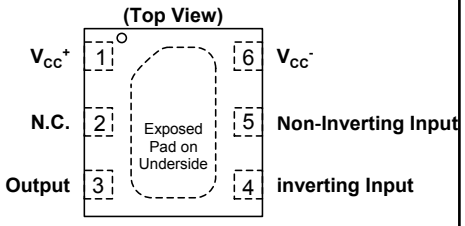
Pin connections



NJM320AF, NJM320AF3



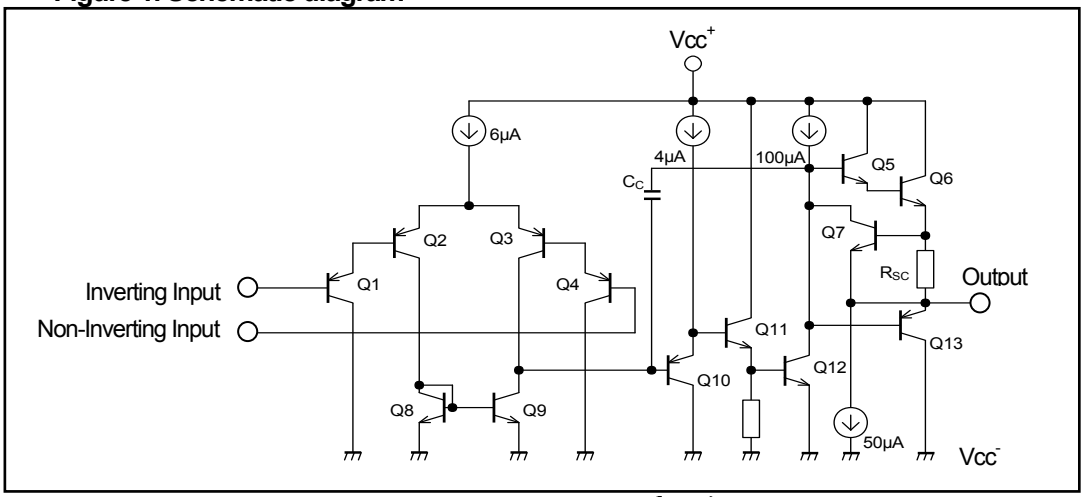
NJM321AF, NJM321AF3



NJM321AKG1(*)
(*)Connect to exposed pad to V_{CC}^-

1 Schematic diagram

Figure 1. Schematic diagram



2 Absolute maximum ratings and operating conditions

Table1. Absolute maximum ratings (Tamb=25ºC)

Symbol	Parameter	RATINGS	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	32	V
V_{IN}	Input voltage (1)	Vcc^- -0.3 to Vcc^- +32	V
V_o	Output Terminal Input Voltage	Vcc^- -0.3 to Vcc^+ +0.3	V
V_{ID}	Differential input voltage	±32	V
I_{IN}	Input current (2)	5mA in DC or 50mA in AC (duty cycle = 10%, T=1s)	mA
T_{stg}	Storage temperature range	-65 to +150	ºC
T_j	Maximum junction temperature	150	ºC
P_D	Power Dissipation	SOT-23-5 : 480(4), 650(5) SC88A : 360(4), 490(5) DFN6-G1 : 330(6), 1200(7)	mW
θja	Thermal resistance junction to ambient(3)	SOT-23-5 : 260(4), 195(5) SC88A : 355(4), 260(5) DFN6-G1 : 385(6), 110(7)	ºC /W
ψjt	Thermal resistance junction to top surface of IC package(3)	SOT-23-5 : 68(4), 58(5) SC88A : 91(4), 74(5) DFN6-G1 : 65(6), 26(7)	ºC /W

1. Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of VCC^+
   The normal amplifier operation input voltage is within "Common Mode Input Voltage Range" specified in the Electrical characteristics.
2. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-vase junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the VCC voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
3. Short-circuit can cause excessive heating and destructive dissipation. Values are typical.
4. Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers FR4)
5. Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers FR4), internal Cu area: 74.2 x 74.2mm
6. Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)
7. Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
   *For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

. Table2. Operating conditions

T_{amb} =25ºC

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	3 to 32	V
T_{oper}	Operating free-air temperature range	-40 to +125	°C

.

3 Electrical characteristics

Table3. V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) T_{amb} = 25°C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 - -	 0.5 -	 2.5 4	mV
DV_{io}	Input offset voltage drift 0 °C ≤ T_{amb} ≤ 70 °C (5)	-	5	30	µV/°C
I_{io}	Input offset current T_{amb} = 25°C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 - -	 2 -	 30 40	nA
DI_{io}	Input offset current drift 0 °C ≤ T_{amb} ≤ 70 °C (5)	-	-	300	pA/°C
I_{ib}	Input bias current (2) T_{amb} = 25°C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 - -	 20 -	 150 200	nA
A_{vd}	Large signal voltage gain (V_{CC}^+ = +15V, R_L=2kΩ, Vo=1.4V to 11.4V) T_{amb} = 25°C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 50 25	 100 -	 - -	V/mV
SVR	Supply voltage rejection ratio(V_{CC}^+ = 5V to 30V, Rs<10kΩ) T_{amb} = 25°C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 65 65	 100 -	 - -	dB
I_{CC}	Supply current, all amp, no load V_{CC}^+ = 5V 0 °C ≤ T_{amb} ≤ 70 °C (5) V_{CC}^+ = 30V 0 °C ≤ T_{amb} ≤ 70 °C (5)	 - -	 0.45 -	 0.7 1	mA
V_{icm}	Input common mode voltage range(V_{CC}^+ = +30V (3)) T_{amb} = 25 °C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 0 0	 - -	 V_{CC}^+ - 1.5 V_{CC}^+ - 2	V
CMR	Common mode rejection ratio(R_S < 10kΩ) T_{amb} = 25°C 0 °C ≤ T_{amb} ≤ 70 °C (5)	 70 60	 100 -	 - -	dB

Table3. V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25˚C , (unless otherwise specified)

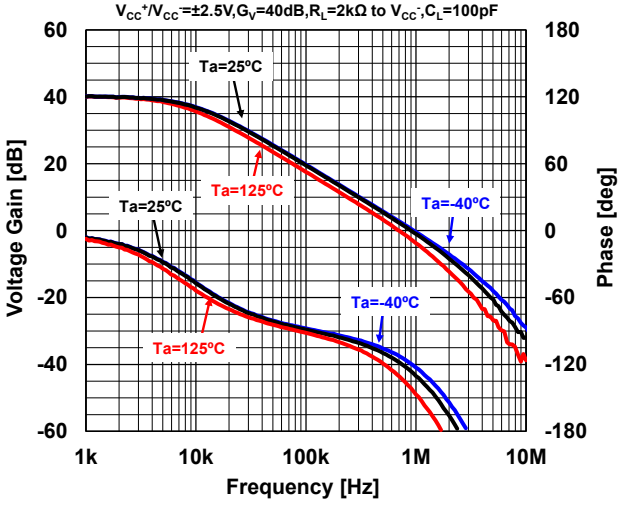
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{source}	Output source current V_{CC}^+ = 15V, V_O = +2V, V_{id} = +1V	20	40	-	mA
I_{sink}	Output sink current V_{CC}^+ = 15V, V_o = +2V, V_{id} = -1V V_{CC}^+ = 15V, V_o = +0.2V, V_{id} = -1V	10 12	20 50	- -	mA µA
V_{OH}	High level output voltage(V_{CC}^+ = 30V) T_{amb} = 25°C,R_L = 2kΩ 0 °C ≤ T_{amb} ≤ 70 °C (5) ,R_L = 2kΩ T_{amb} = 25°C,R_L = 10kΩ 0 °C ≤ T_{amb} ≤ 70 °C (5) ,R_L = 10kΩ	26 26 27 27	27 - 28 -	- - - -	V
V_{OL}	Low level output voltage T_{amb} = 25°C,R_L = 10kΩ 0 °C ≤ T_{amb} ≤ 70 °C (5) ,R_L = 10kΩ	- -	5 -	20 20	mV
SR	Slew rate V_{CC}^+ = 15V, V_i=0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain	-	0.6	-	V/µs
GBP	Gain bandwidth product V_{CC}^+ = 30V, f = 100kHz, V_{in}=10mV, R_L = 2kΩ, C_L = 100pF	-	1.1	-	MHz
THD	Total harmonic distortion f = 1kHz, A_V=20dB, R_L = 2kΩ, V_O = 2V_{pp}, C_L = 100pF	-	0.02	-	%
e_n	Equivalent input noise voltage f = 1kHz, R_S=100Ω, V_{CC}^+ = 30V	-	30	-	nV/√Hz

1. V_O = 1.4V, R_S=0Ω, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V.
2. The direction of the input current is out of the IC.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components, ensure that stray capacitance between these external parts dose not cause coupling.
5. This parameter is not 100% test.

■ TYPICAL CHARACTERISTICS

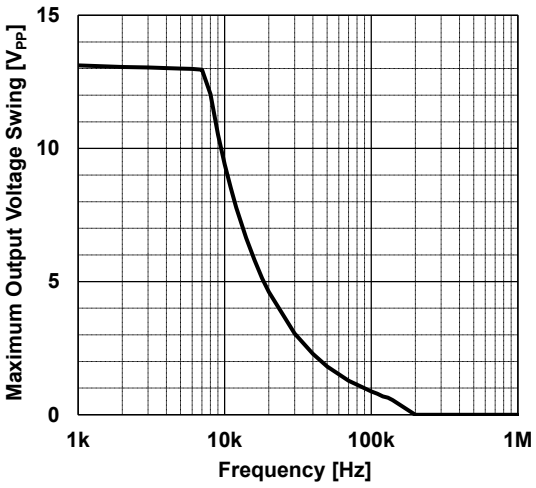
Gain/Phase vs. Frequency

V_{CC}^+/V_{CC}^-=±2.5V,G_V=40dB,R_L=2kΩ to V_{CC}^-,C_L=100pF



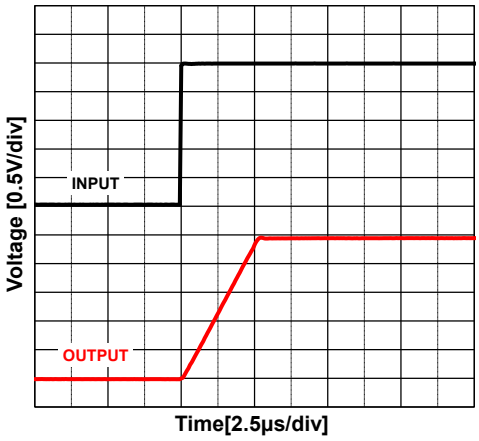
Maximum Output Voltage Swing vs. Frequency

V_{CC}^+=15V, V_{CC}^-=0V,Ta=25°C



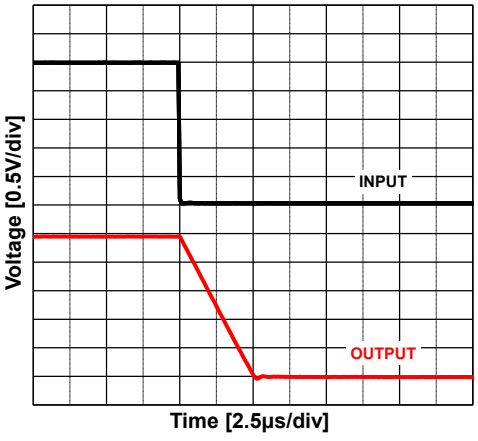
Pulse Response

V_{CC}^+=15V, V_{CC}^-=0V, R_L=2kΩ to V_{CC}^-, C_L=100pF



Pulse Response

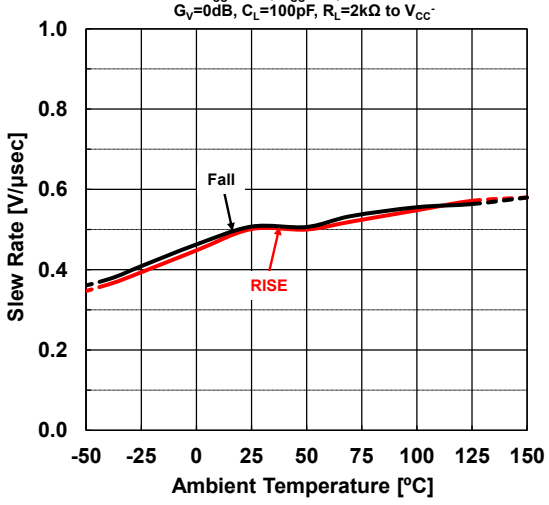
V_{CC}^+=15V, V_{CC}^-=0V, R_L=2kΩ to V_{CC}^-, C_L=100pF



Slew Rate vs. Temperature

V_{CC}^+=15V, V_{CC}^-=0V, f=10kHz

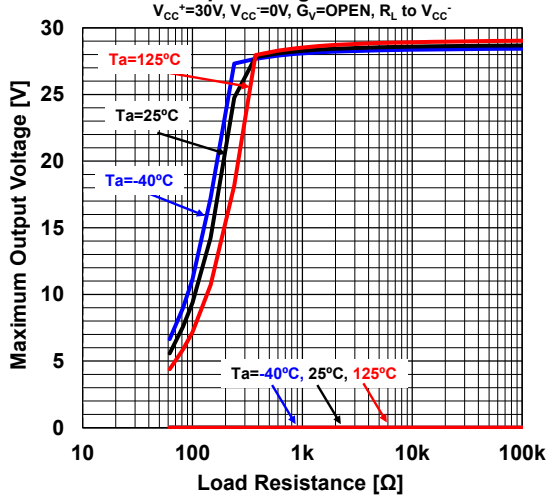
G_V=0dB, C_L=100pF, R_L=2kΩ to V_{CC}^-



■ TYPICAL CHARACTERISTICS

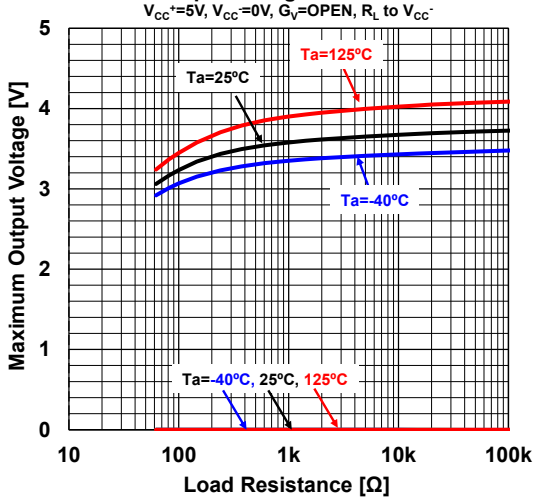
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=30V, V_{CC}^-=0V, G_V=OPEN, R_L to V_{CC}^-



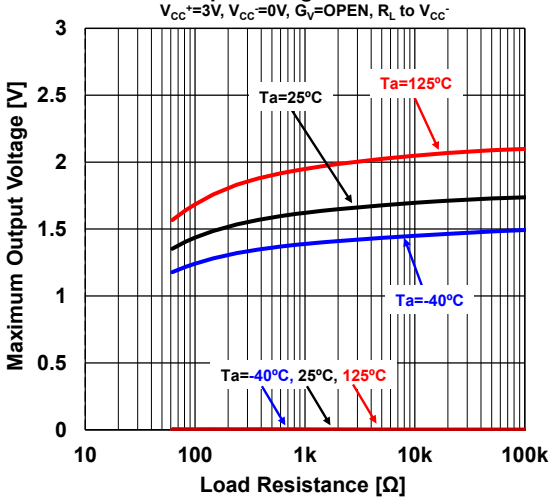
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=5V, V_{CC}^-=0V, G_V=OPEN, R_L to V_{CC}^-



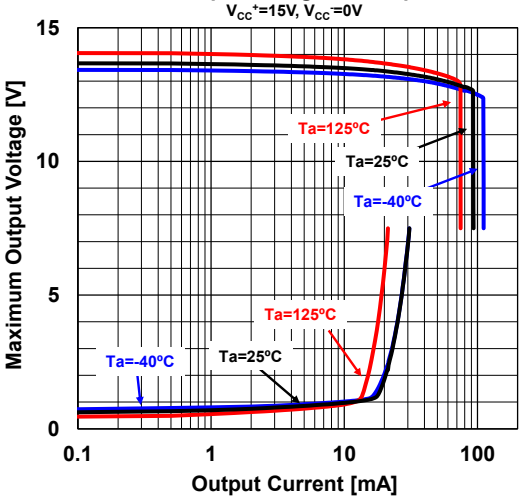
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=3V, V_{CC}^-=0V, G_V=OPEN, R_L to V_{CC}^-



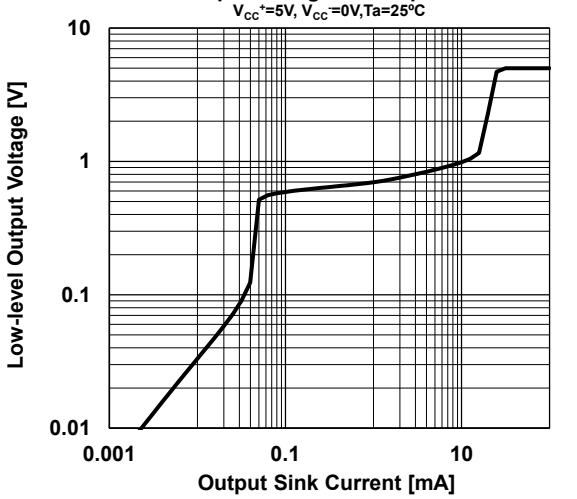
Maximum Output Voltage vs. Output Current

V_{CC}^+=15V, V_{CC}^-=0V



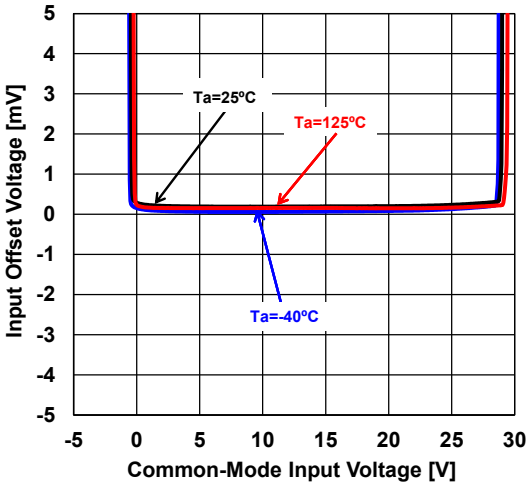
Low-level Output Voltage vs. Output Sink Current

V_{CC}^+=5V, V_{CC}^-=0V,Ta=25°C

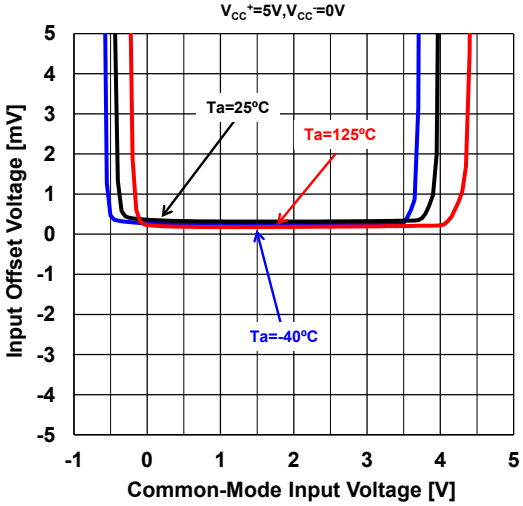


■ TYPICAL CHARACTERISTICS

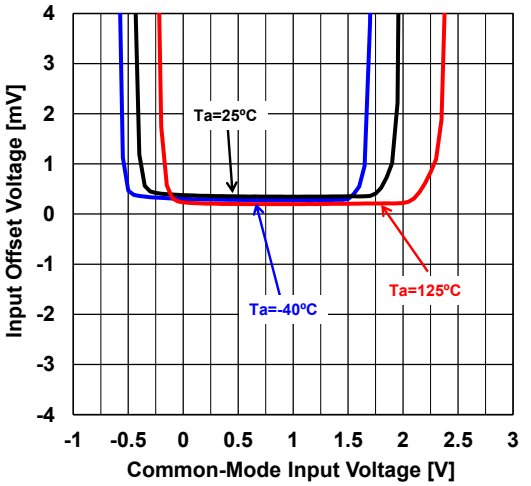
Input Offset Voltage vs. Common-Mode Input Voltage
V_{CC}^+=30V, V_{CC}^-=0V



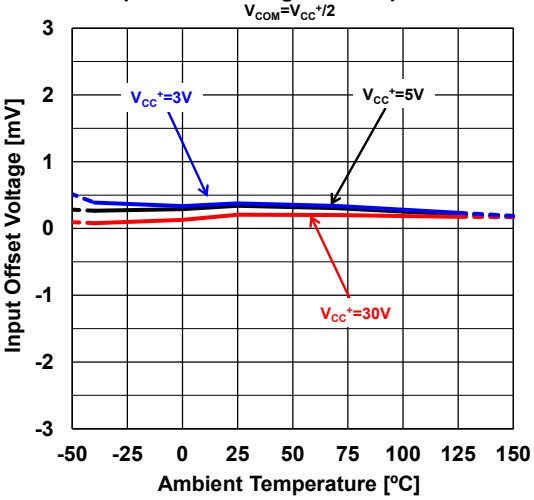
Input Offset Voltage vs. Common-Mode Input Voltage
V_{CC}^+=5V,V_{CC}^-=0V



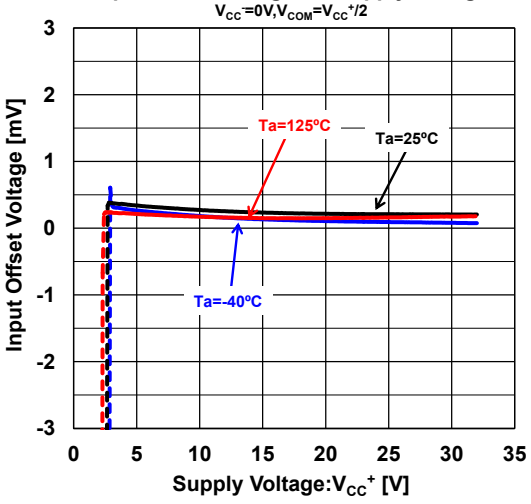
Input Offset Voltage vs. Common-Mode Input Voltage
V_{CC}^+=3V,V_{CC}^-=0V



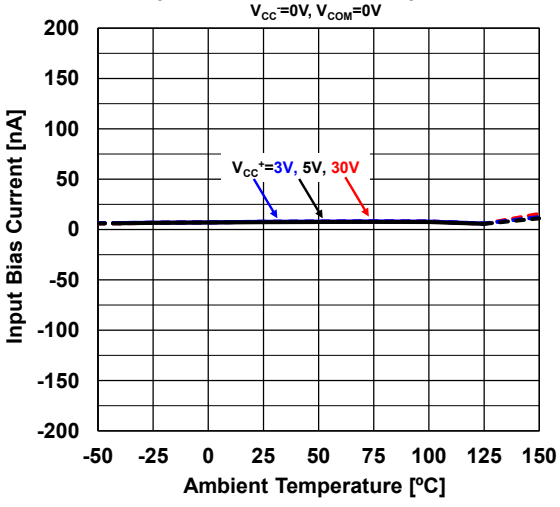
Input Offset Voltage vs. Temperature
V_{COM}=V_{CC}^+/2



Input Offset Voltage vs. Supply Voltage
V_{CC}^-=0V,V_{COM}=V_{CC}^+/2



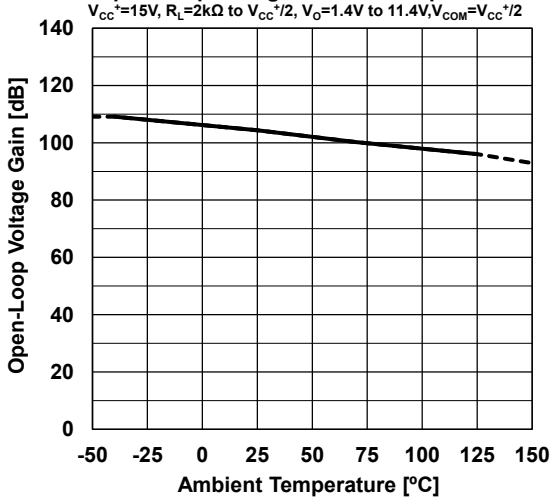
Input Bias Current vs. Temperature
V_{CC}^-=0V, V_{COM}=0V



■ TYPICAL CHARACTERISTICS

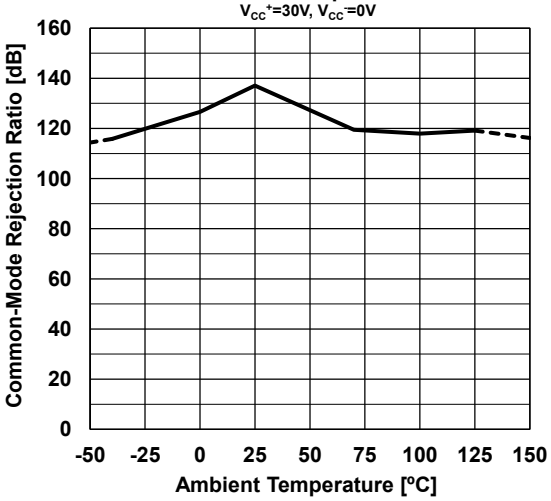
Open-Loop Voltage Gain vs. Temperature

V_{CC}^+=15V, R_L=2kΩ to V_{CC}^+/2, V_O=1.4V to 11.4V, V_{COM}=V_{CC}^+/2



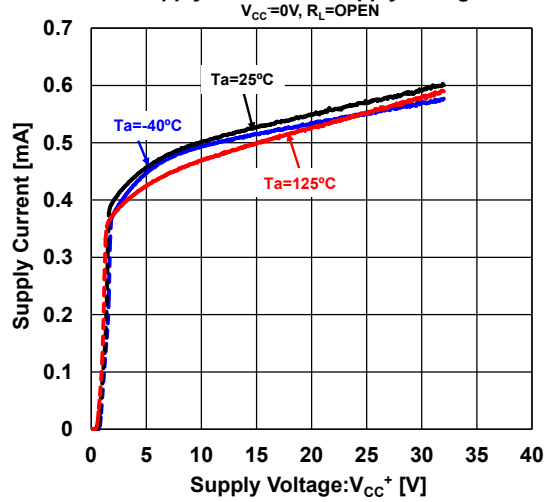
CMR vs. Temperature

V_{CC}^+=30V, V_{CC}^-=0V



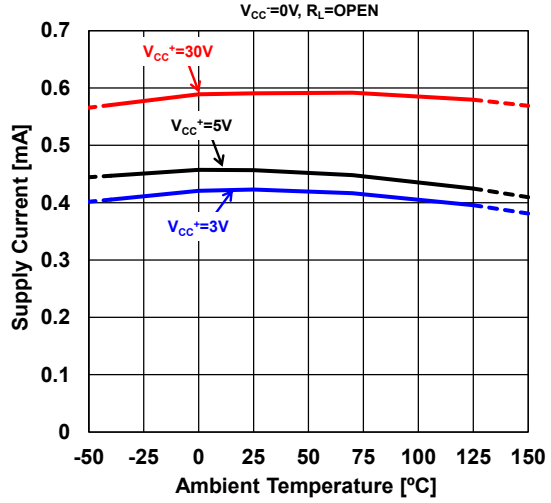
Supply Current vs. Supply Voltage

V_{CC}^-=0V, R_L=OPEN



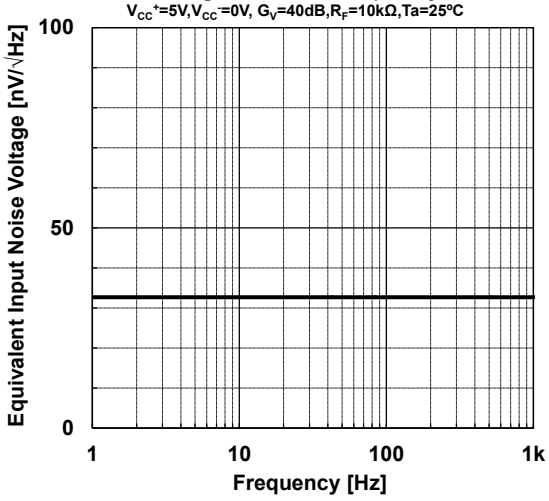
Supply Current vs. Temperture

V_{CC}^-=0V, R_L=OPEN



Voltage Noise vs. Frequency

V_{CC}^+=5V, V_{CC}^-=0V, G_V=40dB, R_F=10kΩ, Ta=25ºC



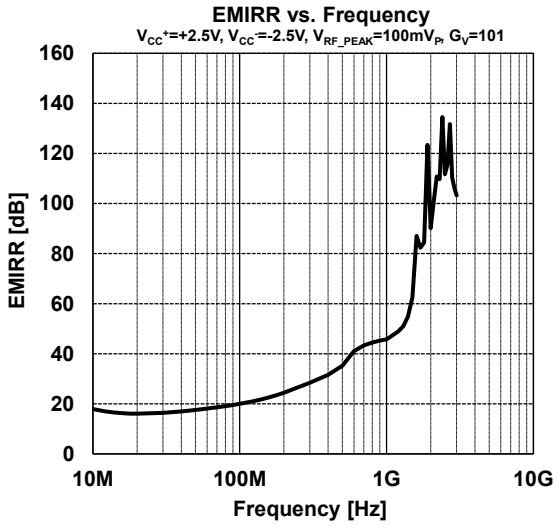
■APPLICATION NOTE

EMIRR(EMI Rejection Ratio) Definition

EMIRR is a parameter indicating the EMI robustness of an OP-Amp. The definition of EMIRR is given by the following a formula (1). We can grasp the tolerance of the RF signal by measuring an RF signal and offset voltage shift quantity.
Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

$$EMIRR = 20 \cdot \log\left(\frac{V_{RF\_PEAK}}{|\Delta V_{IO}|}\right) \quad \cdots(1)$$

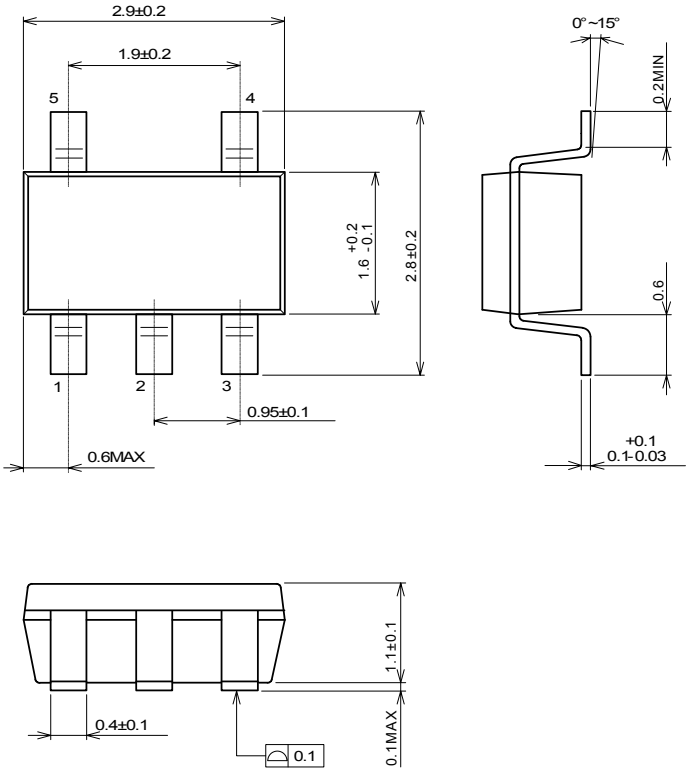
V_{RF_PEAK} : RF Signal Amplitude [V_P]
ΔV_{IO} : Input offset voltage shift quantity [V]



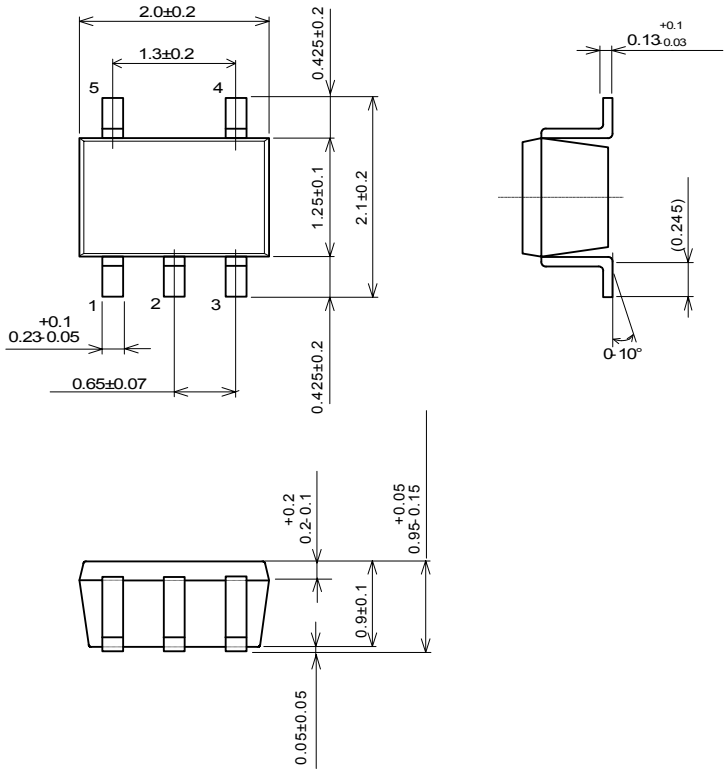
*For details, refer to " Application Note for EMI Immunity" in our HP: http://www.njr.com/

■PACKAGE OUTLINE UNIT : mm

SOT-23-5



SC-88A



■PACKAGE OUTLINE UNIT : mm

DFN6-G1 (ESON6-G1)