1.5A Fixed Voltage LDO Linear Regulator

General Description

The EMP8110 is a CMOS low-dropout linear regulator that operates in the input voltage range from +2.5V to +6.5V and delivers 1.5A output current.

The EMP8110 features include fault detection, bandgap voltage reference, short-circuit protection and thermal shutdown protection. The EMP8110 series devices are available in E-SOP-8L and SOT-223 packages.

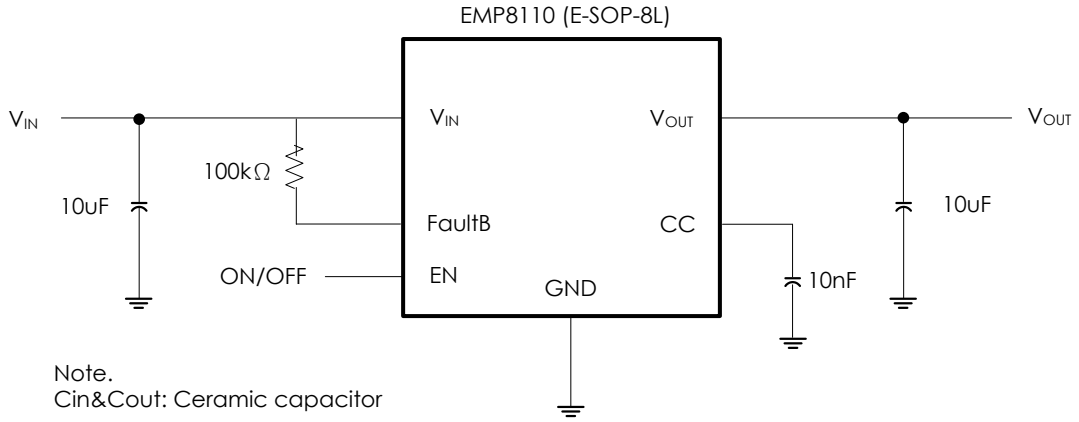
Applications

- High Efficiency Linear Regulators
- Monitor Microprocessors
- Low Voltage Micro-Controllers
- Post Regulator for Switching Power

Features

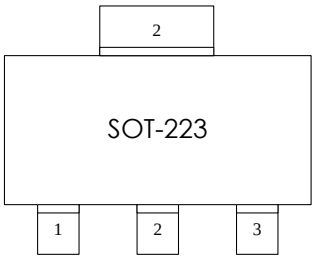
- Operating Voltage Range：+2.5V to +6.5V
- Output Voltages：+1.2V to +4.5V (0.1V Step)
- Maximum Output Current：1.5A
- Dropout Voltage：570mV @ 1.5A(Vout=1.8V)
- Low Current Consumption：65μA (Typ.)
- ±2% Output Voltage Accuracy
- 45μs typical fast turn-on time (Vout=3.3V)
- Low ESR Capacitor Compatible
- High Ripple Rejection：60 dB (Vout=1.8V)
- Fold back short circuit protection
- Thermal Overload Shutdown Protection
- E-SOP-8L and SOT-223 Packages
- RoHS Compliant and 100% Lead (Pb)-Free and Green (Halogen Free with Commercial Standard)

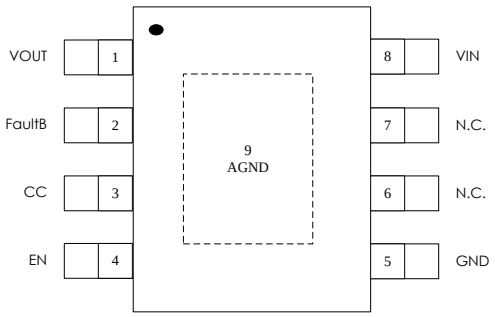
Typical Application



Note.
Cin&Cout: Ceramic capacitor

Connection Diagrams





Order Information

EMP8110-XXVE#3NRR

XX Output voltage

VE#3 SOT-223 Package (Package Code)

: Pin fuction type

NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85°C

Package in Tape & Reel

EMP8110-XXSG08NRR

XX Output voltage

SG08 E-SOP-8L Package (Package Code)

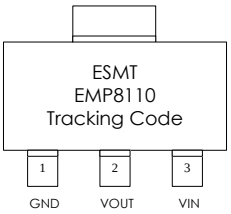
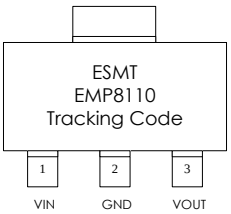
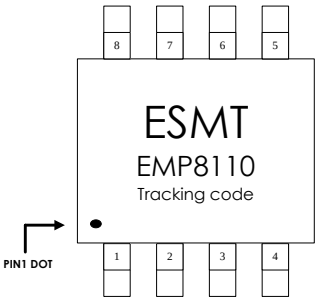
NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85°C

Package in Tape & Reel

Order, Marking & Packing Information

Package	Vout	Product ID.	Marking	Packing
SOT-223	1.2-4.5V	EMP8110-XXVEJ3NRR		Tape & Reel 2.5kpcs
SOT-223	1.2-4.5V	EMP8110-XXVEG3NRR		Tape & Reel 2.5kpcs
E-SOP-8L	1.2-4.5V	EMP8110-XXSG08NRR		Tape & Reel 3kpcs

Note.

XX: Output voltage, example

12: 1.2V output

25: 2.5V output

Pin Functions

Name	E-SOP-8L	SOT-223		Function
		J	G	
VOUT	1	2	3	**Output Voltage.**
FaultB	2	N/A	N/A	**Fault Detection Output.** The FaultB pin goes low when the voltage regulating function fails. Because the FaultB pin connects to the open-drain output of a NMOS transistor, a typical 100kohm pull-up resistor is required to provide the necessary output voltage.
CC	3	N/A	N/A	**Compensation Capacitor.** Connect an optimum 10nF noise bypass capacitor between the CC and the ground pins to reduce noise in VOUT.
EN	4	N/A	N/A	**Shutdown Input.** To keep the regulator on during normal operation, connect the EN pin to VIN. Set the regulator into the disable mode by pull in the EN pin to GND. The EN pin must not exceed VIN under all operating conditions.
GND	5	1	2	**Ground Pin.**
N.C.	6, 7	N/A	N/A	**Not connected.**
VIN	8	3	1	**Supply Voltage Input.** Require a minimum input capacitor of close to 10μF to ensure stability and sufficient decupling from the ground pin.

Functional Block Diagram

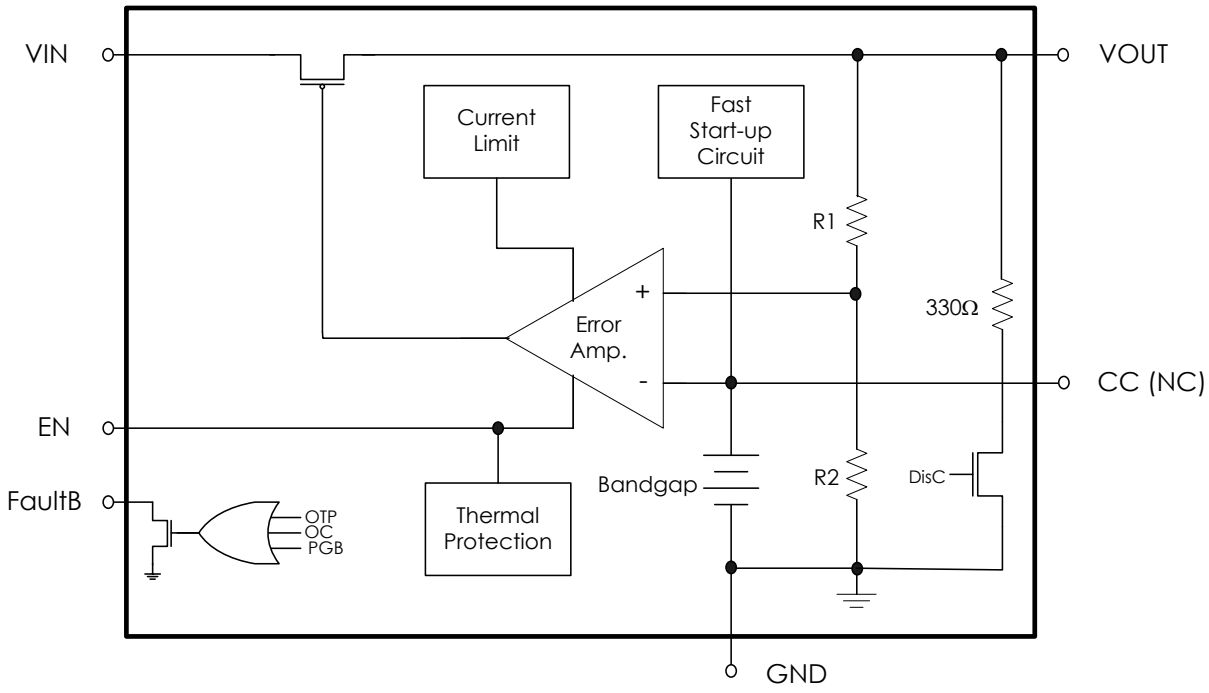


FIG.1. Functional Block Diagram of EMP8110

Absolute Maximum Ratings (Notes 1, 2)

IN	-0.3V to 7V	Junction Temperature (T_J)	155°C
OUT	-0.3V to 5.0V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 8)	ESD Rating	
Storage Temperature Range	-55°C to 150°C	Human Body Model	2KV

Operating Ratings (Note 1, 2)

Supply Voltage	2.5V to 6.5V	- SOT-223 (package code VEG3)	55°C/W
Operating Temperature Range	-40°C to 85°C	- SOT-223 (package code VEJ3)	70°C/W
Thermal Resistance (θ_{JA} , Note 3))			
- E-SOP-8L	40°C/W		

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT}+1V, C_{IN} = C_{OUT} = 10μF, T_A = 25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.5		6.5	V
V_{OUT}	Output Accuracy	V_{IN}=V_{OUT}+1V, I_{OUT}=10mA	-2%	V_{OUT}	+2%	V
I_{MAX}	Output Current		1.5			A
I_{LIMIT}	Current Limit			1.8		A
V_{DROP}	Dropout Voltage	I_{OUT}= 1000mA, 2.5V<V_{OUT}≦4.5V		270		mV
		I_{OUT}= 1000mA, 1.5<V_{OUT}≦2.5V		330	600	mV
		I_{OUT}= 1000mA, 1.4<V_{OUT}≦1.5V		380	800	mV
		I_{OUT}= 1000mA, 1.3<V_{OUT}≦1.4V		450	900	mV
		I_{OUT}= 1000mA, 1.2<V_{OUT}≦1.3V		500	1000	mV
ΔV_{LINE}	Line Regulation	V_{OUT}≦2V, 2.5V≦V_{in}≦3 V, I_{OUT}=30mA	-0.15	0.1	0.15	%/V
		V_{OUT} +1V≦V_{in}≦V_{out} +2, I_{OUT}=30mA	-0.1	0.02	0.1	%/V
ΔV_{LOAD}	Load Regulation	V_{IN}=V_{OUT}+1V, 1mA≦I_{OUT}≦1500mA		0.02	0.05	%/mA
I_Q	Ground Pin Current	I_{LOAD}=0mA, V_{IN} = V_{OUT}+1.0V		65		μA
		I_{LOAD}=1000mA, V_{IN} = V_{OUT}+1.0V		90		μA
		I_{LOAD}=1500mA, V_{IN} = V_{OUT}+1.0V		115		μA
I_{SC}	Fold back Short Circuit Current			250		mA
PSRR	Ripple Rejection	I_{OUT}=100mA @1kHz, V_{OUT}=1.8V		60		dB
e_n	Output Voltage Noise	C_{CC}=10nF, I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz		110		μV_{RMS}
VEN	EN Input Threshold	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V	1.2			V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V			0.4	
IEN	EN Input Bias Current	EN = GND or V_{IN}=5.5V			1	μA
V_{FaultB}	FaultB Output Threshold	Sink 4mA			0.4	V

T_{SD}	Thermal Shutdown Temperature			160		°C
T_{HYS}	Thermal Shutdown Hysteresis			30		°C
T_{ON}	Start-Up Time	V_{OUT}=3.3V, C_{OUT}=10μF, V_{OUT} at 90% of Final Value		50		μs
		V_{OUT}=3.3V, C_{OUT}=10μF, C_{CC}=10nF, V_{OUT} at 90% of Final Value		145		

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a high effective thermal conductivity test board (ESMT EVB, 2 layers PCB, 1S1P).

Note 4: Condition does not apply to input voltages below 2.2V since this is the minimum input operating voltage.

Note 5: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 1V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.2V.

Note 6: Turn-off time is time measured between the enable input just decreasing below V_{IL} and the output voltage just decreasing to 10% of its nominal value.

Note 7: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

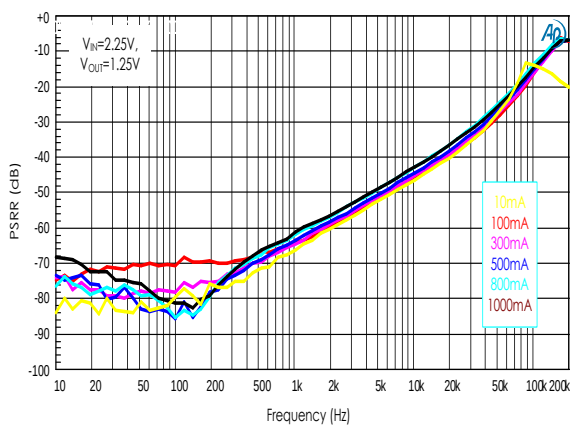
Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-223 packageθ_{JA} = 55°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 2.27W. The derating factor (-1/θ_{JA}) = -18.18mW/°C, thus below 25°C the power dissipation figure can be increased by 18.18mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 8: Typical Values represent the most likely parametric norm.

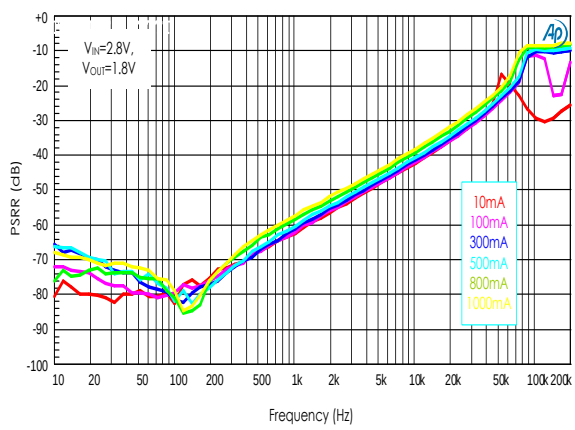
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = C_{OUT} = 10μF, T_A = 25°C

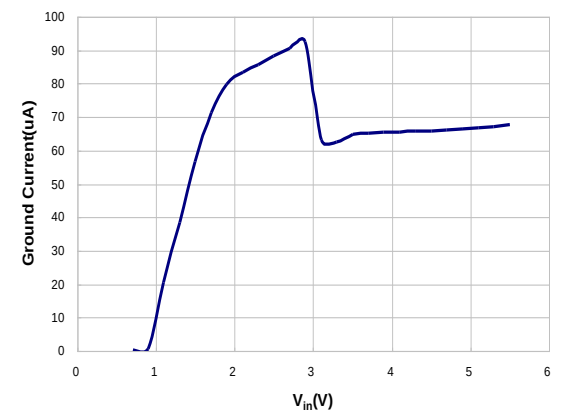
PSRR vs. Frequency (V_{OUT}=1.25V)



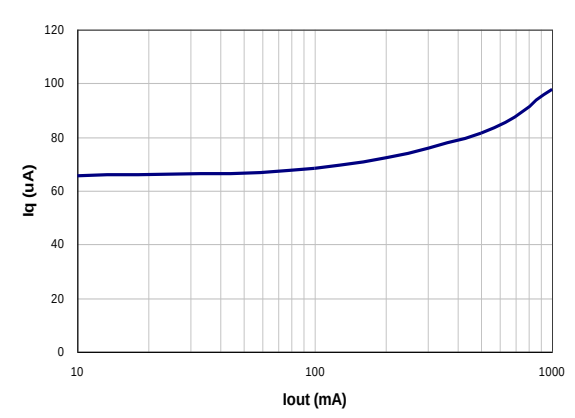
PSRR vs. Frequency (V_{OUT}=1.8V)



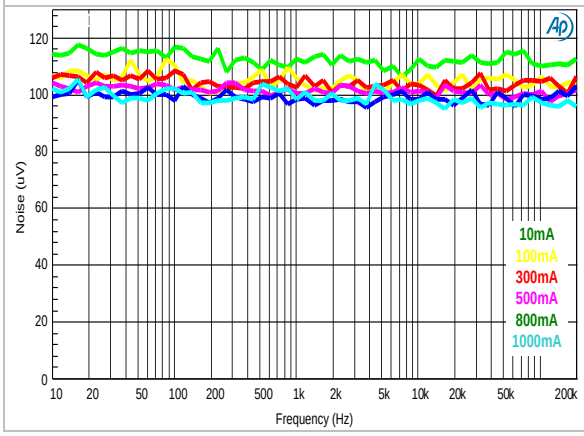
Ground Current vs. V_{IN} (V_{OUT}=3.3V)



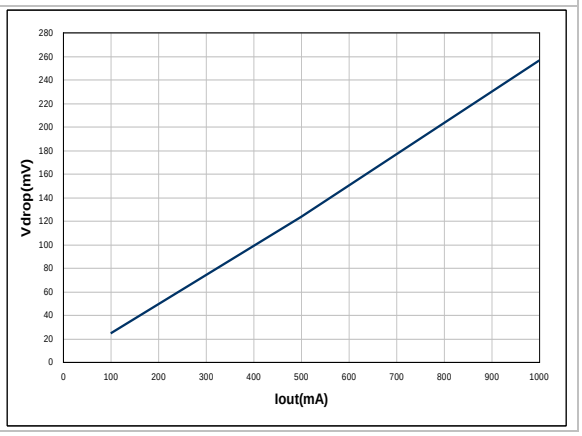
Ground Current vs. I_{OUT} (V_{OUT}=3.3V)



Output Voltage Noise (V_{OUT}=3.3V)



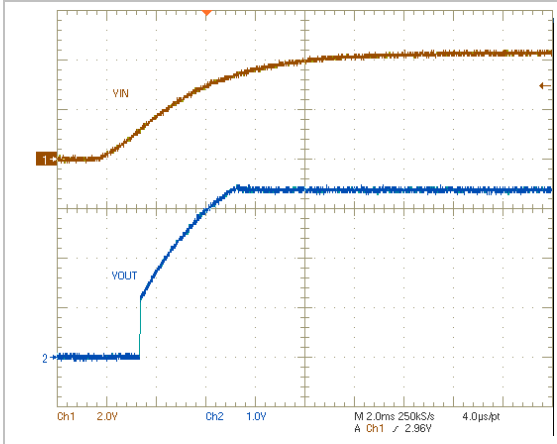
Dropout Voltage (V_{OUT}=3.3V)



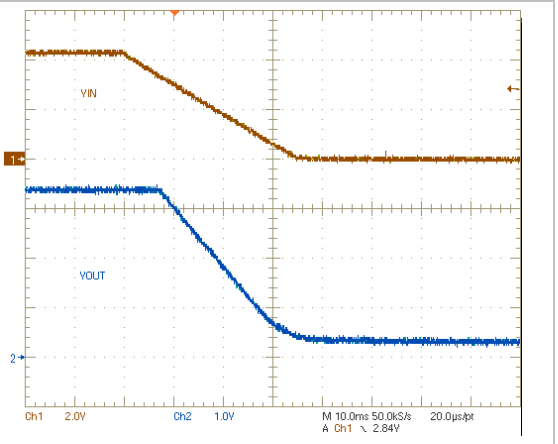
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = C_{OUT} = 10μF, T_A = 25°C

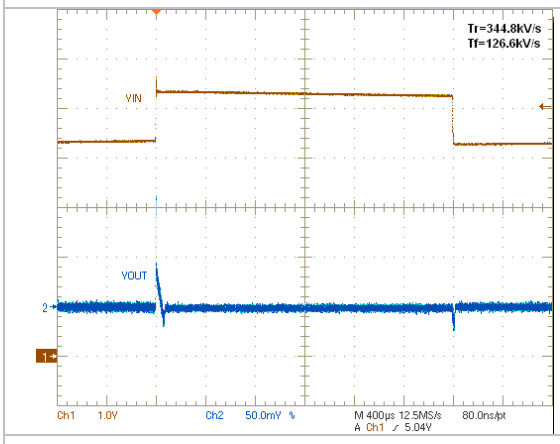
Power On Response (V_{OUT}=3.3V)



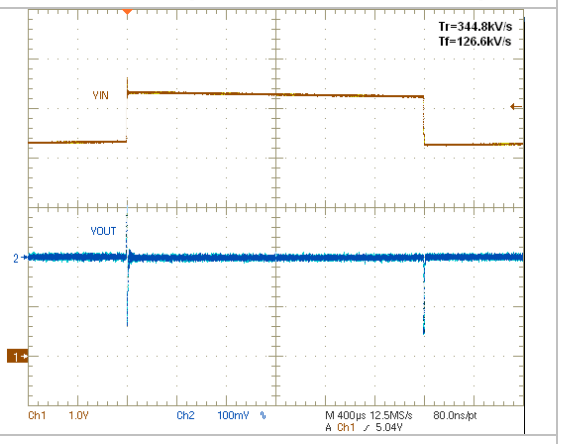
Power Off Response (V_{OUT}=3.3V)



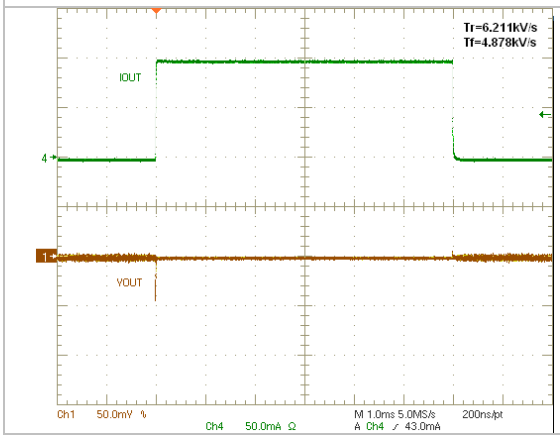
Line transient (Vin=4.3V~5.3V, Iout=1mA)



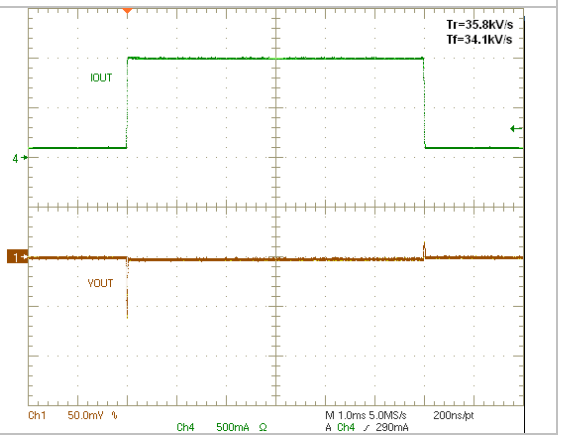
Line transient (Vin=4.3V~5.3V, Iout=100mA)



Load transient (V_{OUT}=3.3V, I_{OUT}=1mA to 100mA)



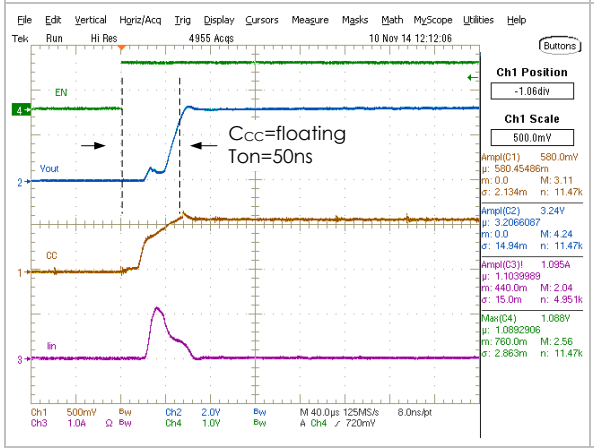
Load transient (V_{OUT}=3.3V, I_{OUT}=100mA to 1A)



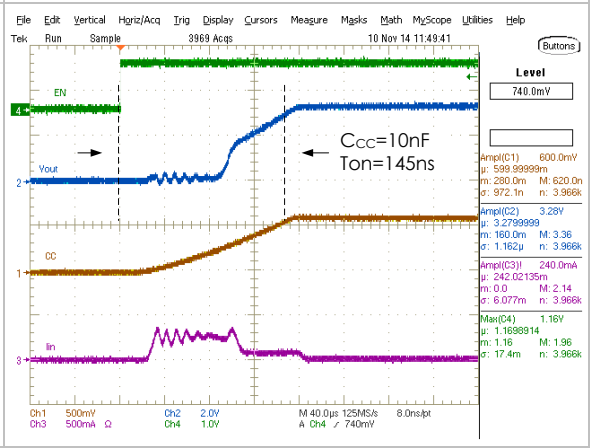
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = C_{OUT} = 10μF, T_A = 25°C

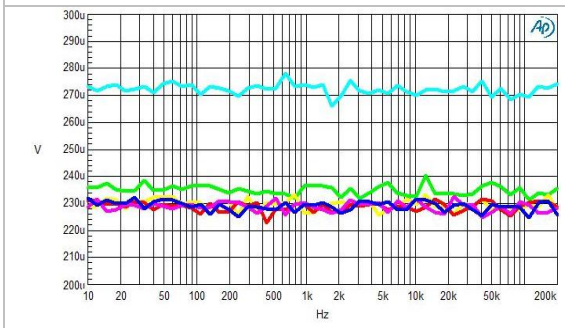
Enable Response, C_{CC}=floating (V_{OUT}=3.3V)



Enable Response, C_{CC}=10nF (V_{OUT}=3.3V)

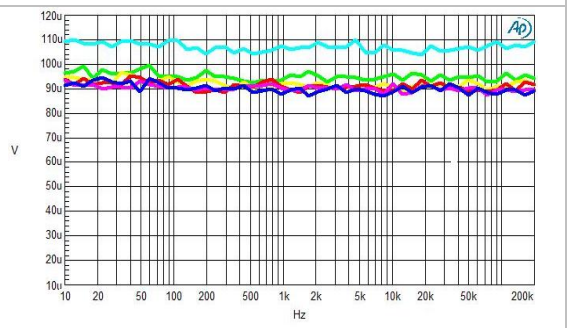


Noise Level, C_{CC}=floating (V_{OUT}=3.3V)



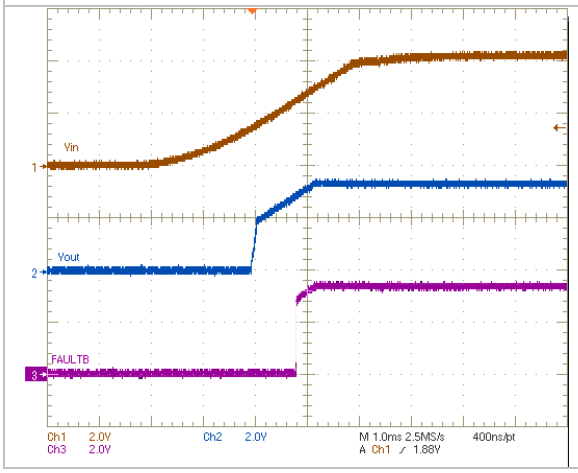
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	4	Anlr.Ampl	Left	SN2,without CC, Iout=10mA
2	1	Green	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=100mA
3	1	Yellow	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=300mA
4	1	Red	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=500mA
5	1	Magenta	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=800mA
6	1	Blue	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=1000mA

Noise Level, C_{CC}=10nF (V_{OUT}=3.3V)

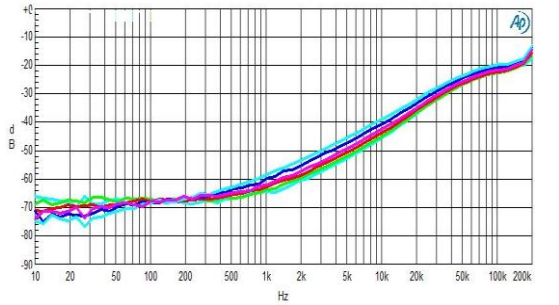


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=10mA
2	1	Green	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=100mA
3	1	Yellow	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=300mA
4	1	Red	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=500mA
5	1	Magenta	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=800mA
6	1	Blue	Solid	4	Anlr.Ampl	Left	SN2,CC=10nF Iout=1000mA

FaultB Pin State (V_{OUT}=3.3V)



PSRR, C_{CC}=10nF (V_{OUT}=3.3V)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Anlr.Crosstalk	Left	SN.1 Vin=4.3V, Vout=3.3V, C.C=10nF, Iout=10mA
2	1	Green	Solid	3	Anlr.Crosstalk	Left	SN.1 Vin=4.3V, Vout=3.3V, C.C=10nF, Iout=100mA
4	1	Red	Solid	3	Anlr.Crosstalk	Left	SN.1 Vin=4.3V, Vout=3.3V, C.C=10nF, Iout=300mA
5	1	Magenta	Solid	3	Anlr.Crosstalk	Left	SN.1 Vin=4.3V, Vout=3.3V, C.C=10nF, Iout=500mA
6	1	Blue	Solid	3	Anlr.Crosstalk	Left	SN.1 Vin=4.3V, Vout=3.3V, C.C=10nF, Iout=800mA
7	1	Cyan	Solid	3	Anlr.Crosstalk	Left	SN.1 Vin=4.3V, Vout=3.3V, C.C=10nF, Iout=1000mA

Application Information

Detail Description

The EMP8110 is a CMOS low-dropout linear regulator. The device provides fixed output voltages for output current up to 1.5A. The band-gap reference voltage is connected to the error amplifier, which compares this reference with the feedback voltage and amplifies the voltage difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, which allows more current to pass to the output pin and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up to decrease the output voltage. The output voltage is fed back through an internal resistive divider connected to OUT pin. Additional blocks include an output current limiter, thermal sensor, and shutdown logic.

Internal P-channel Pass Transistor

The EMP8110 features a P-channel MOSFET pass transistor. Unlike similar designs using PNP pass transistors, P-channel MOSFETs require no base drive, which reduces quiescent current. PNP-based regulators also waste considerable current in dropout when the pass transistor saturates, and use high base-drive currents under large loads. The EMP8110 does not suffer from these problems and consumes only 65μA (Typ.) of current consumption.

Output Voltage Selection

For voltage type of EMP8110, the output voltage is preset at an internally trimmed voltage. The first two digits of part number suffix identify the output voltage (see Ordering Information). For example, the EMP8110-33 has a preset 3.3V output voltage.

Dropout Voltage

A regulator's minimum input-output voltage differential, or dropout voltage, determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. The EMP8110 use a P-channel MOSFET pass transistor, its dropout voltage is a function of drain-to-source on-resistance RDS(ON) multiplied by the load current.

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Current Limit

The EMP8110 also includes a fold back current limiter. It monitors and controls the pass transistor's gate voltage, estimates the output current, and limits the output current within 1.8A (Typ.).

Shutdown

The EMP8110 enters the shutdown mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to <1uA. Such a low supply current makes the EMP8110 best suited for battery-powered applications.

Fault Detection

In the event of the occurrence of various fault conditions that cause failure in the output voltage regulation, such as during thermal overload or current limit, the FaultB pin of the EMP8110 becomes low. Because the FaultB pin connects to the open-drain output of a N-channel MOS transistor, a large pull-up resistor 100kohm (typical) is required to provide the necessary output voltage and without compromising the overall power consumption performance of the regulator.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the EMP8110. When the junction temperature exceeds T_J = +160°C, a thermal sensor turns off the pass transistor, allowing the IC to cool down. The thermal sensor turns the pass transistor on again after the junction temperature cools down by 30°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection is designed to protect the EMP8110 in the event of fault conditions. For continuous operation, the absolute maximum operating junction temperature rating of T_J = +125°C should not be exceeded.

Fast Start-Up

Fast start-up time is important for overall system efficiency improvement. The EMP8110 assures fast start-up speed when without using the optional noise bypass capacitor (CC). To shorten start-up time, the EMP8110 internally supplies a current to charge up the capacitor until it reaches about 90% of its final value.

Output Capacitor

The EMP8110 is specially designed for use with ceramic output capacitors of as low as 10μF to take advantage of the savings in cost and space, as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω . The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8110 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8110 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 10μF is required for EMP8110. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout.

Compensation (Noise Bypass) Capacitor

Substantial reduction in the output voltage noise of the EMP8110 is accomplished by connecting the noise bypass capacitor (10nF) between CC pin and the ground. Because CC pin connects directly to the high impedance output of the bandgap reference circuit, the level of the DC leakage currents in the CC capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the CC capacitor types for use with the EMP8110. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the CC capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Trade off exists between output noise level and turn-on time when selecting the CC capacitor value.

Operating Region and Power Dissipation

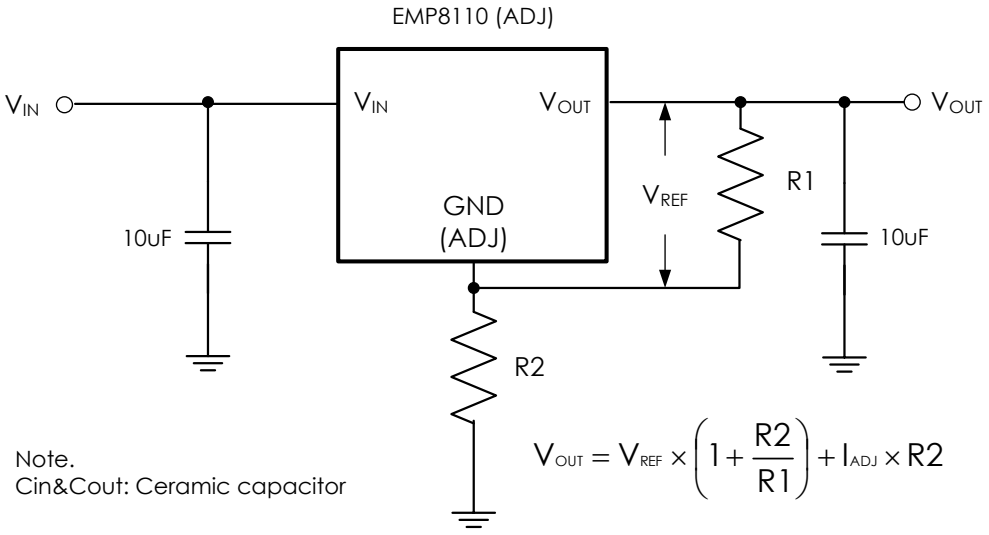
Maximum power dissipation of the EMP8110 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the devices is $P = I_{OUT} \times (V_{IN}-V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = \frac{(T_J - T_A)}{\theta_{JC} + \theta_{CA}} = \frac{(T_J - T_A)}{\theta_{JA}}$$

Where (T_J-T_A) is the temperature difference between the EMP8110 die junction and the surrounding air, θ_{JC} is the thermal resistance of the package chosen, and θ_{CA} is the thermal resistance through the printed circuit board, copper traces and other materials to the surrounding air. For better heat-sinking, the copper area should be equally shared between the IN, OUT, and GND pins.

Application Circuit

a) Application circuit for adjustment V_{OUT}



Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to GND (ADJ) pin. The regulated voltage is V_{REF} between V_{OUT} and GND (ADJ) pin. Thus the output voltage is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \times R2$$

R2 recommended value is 1kΩ, Table 1 lists recommended values of R1 and R2 for most used output voltage.

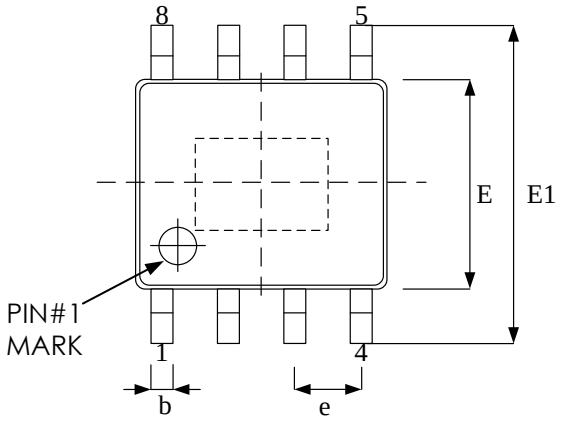
Table 1. Recommended Resistance Values

V_{OUT}	Output Version	V_{REF}	I_{ADJ}	R1	R2
3.3V	1.2V	1.2V	65uA	0.59 kΩ	1 kΩ
2.8V	1.2V	1.2V	65uA	0.78 kΩ	1 kΩ
2.5V	1.2V	1.2V	65uA	0.97 kΩ	1 kΩ
1.8V	1.2V	1.2V	65uA	2.24 kΩ	1 kΩ
1.5V	1.2V	1.2V	65uA	5.11 kΩ	1 kΩ
3.3V	1.8V	1.8V	65uA	1.25 kΩ	1 kΩ
2.5V	1.8V	1.8V	65uA	2.83 kΩ	1 kΩ

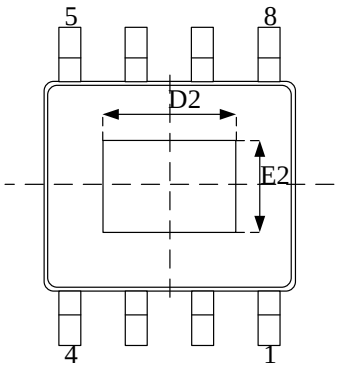
Note.

The load regulation performance degradation can be expected during ADJ application if R2 value too large adopted.

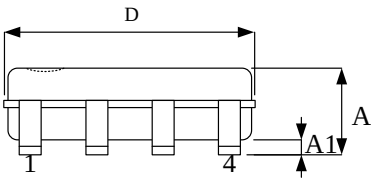
Package Outline Drawing
SOP-8 (E) (150 mil)



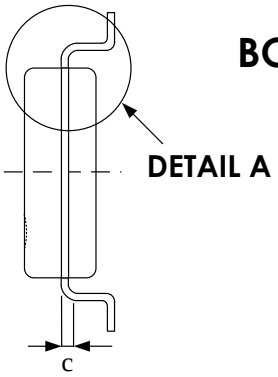
TOP VIEW

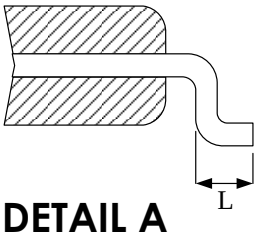


BOTTOM VIEW



SIDE VIEW





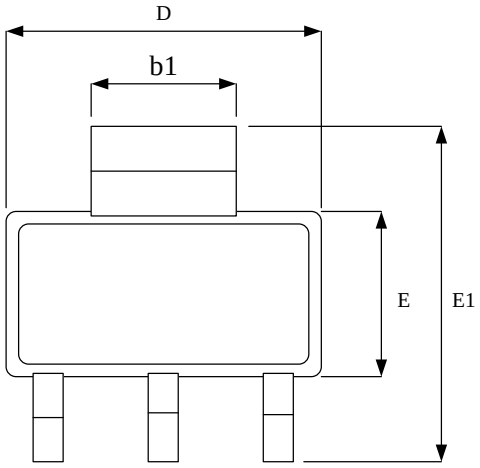
DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	1.35	1.75
A1	0.00	0.25
b	0.33	0.51
c	0.17	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.41	1.27

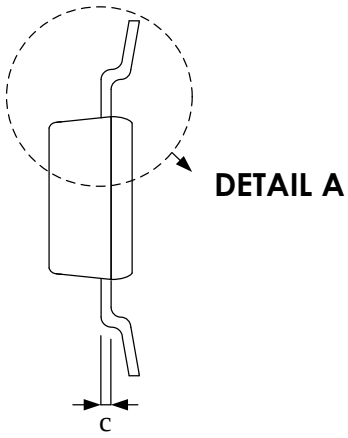
Exposed pad

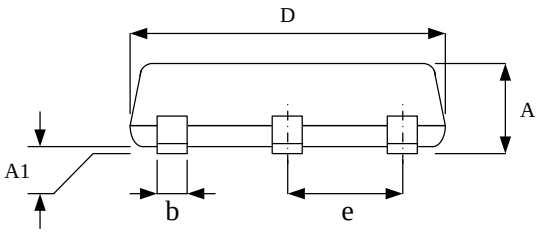
	Dimension in mm	
	Min	Max
D2	1.93	2.39
E2	1.93	2.39

Package Outline Drawing
SOT-223

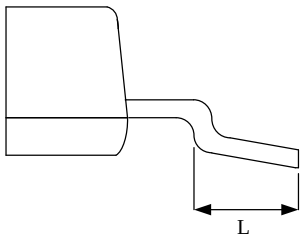


TOP VIEW





SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	--	1.80
A1	0.02	0.10
b	0.60	0.80
b1	2.90	3.10
c	0.23	0.35
D	6.30	6.80
E	3.30	3.70
E1	6.70	7.30
e	2.30 BSC	
L	0.90	--

Revision History

Revision	Date	Description
0.1	2013.07.01	Initial version.
0.2	2013.11.13	1) Added ADJ application circuit. 2) Removed EMP logo and update marking information.
0.3	2014.07.01	1) Updated Q_{JA} information. 2) Revised note. 3 information. 3) Removed TBX and VEX package option. 4) Updated TBG and TBJ Packing information.
0.4	2014.07.28	1) Modify Electrical Characteristics VOUT Parameter. 2) Revise the Order,Marking & Packing Information.
0.5	2014.11.21	Added E-SOP-8L package option into.
1.0	2015.03.11	Revise version to 1.0 & remove preliminary word
1.1	2015.04.24	Delete TO-252 package

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