CT427

XtremeSense® TMR Ultra-Low Noise, <1% Total Error Current Sensor

Features

- Integrated Contact Current Sensing for Low to Medium Current Ranges:
  - -20 A to +20 A
  - -30 A to +30 A
- Integrated Current Carrying Conductor (CCC)
- Linear Analog Output Voltage
- Total Error Output ≤ ±1.0% FS
- 1 MHz Bandwidth
- Response Time: ~0.30 µs
- Supply Voltage: 3.0 V to 3.6 V
- Low Noise: 10 mA_{RMS} to 12 mA_{RMS} @ f_{BW} = 100 kHz
- Filter Function to Reduce Noise on Output Pin
- Immunity to Common Mode Fields: <5.0 mA/mT
- Supply Voltage: 3.0 V to 3.6 V
- Over-Current Detection (OCD™)
  - Out of Range Currents
- 8-Lead SOIC Package

Applications

- Solar/Power Inverters
- UPS, SMPS and Telecom Power Supplies
- Battery Management Systems
- Motor Control
- White Goods
- Consumer and Enterprise Electronics
- Over-Current Fault Protection

Product Description

The CT427 is a high bandwidth and ultra-low noise integrated contact current sensor that uses Crocus Technology's patented XtremeSense® TMR technology to enable high accuracy current measurements for many consumer, enterprise, and industrial applications. It supports two (2) current ranges where the integrated current carrying conductor (CCC) will handle up to 30 A of current and generates a current measurement as a linear analog output voltage. It achieves a total output error of less than ±1.0% full-scale (FS).

It has about a 0.30 µs output response time while the current consumption is about 6.0 mA and is immune to common mode fields. The CT427 has an integrated over-current detection (OCD) circuitry to identify out of range currents (OCD) with the result outputted to the fault-bar ($\overline{FLT}$) pin. The $\overline{FLT}$ is an open drain, active LOW digital signal that is activated by the CT427 to alert the microcontroller that a fault condition has occurred.

The CT427 is offered in an industry standard 8-lead SOIC package that is "green" and RoHS compliant.

Part Ordering Information

Part Number	Operating Temperature Range	Current Range	Package	Packing Method
CT427-ESN820MR	-40°C to +85°C	-20 A to +20 A	8-lead SOIC 4.89 x 6.00 x 1.47 mm	Tube
CT427-HSN820MR	-40°C to +125°C			
CT427-ESN830MR	-40°C to +85°C	-30 A to +30 A		
CT427-HSN830MR	-40°C to +125°C			

Block Diagram

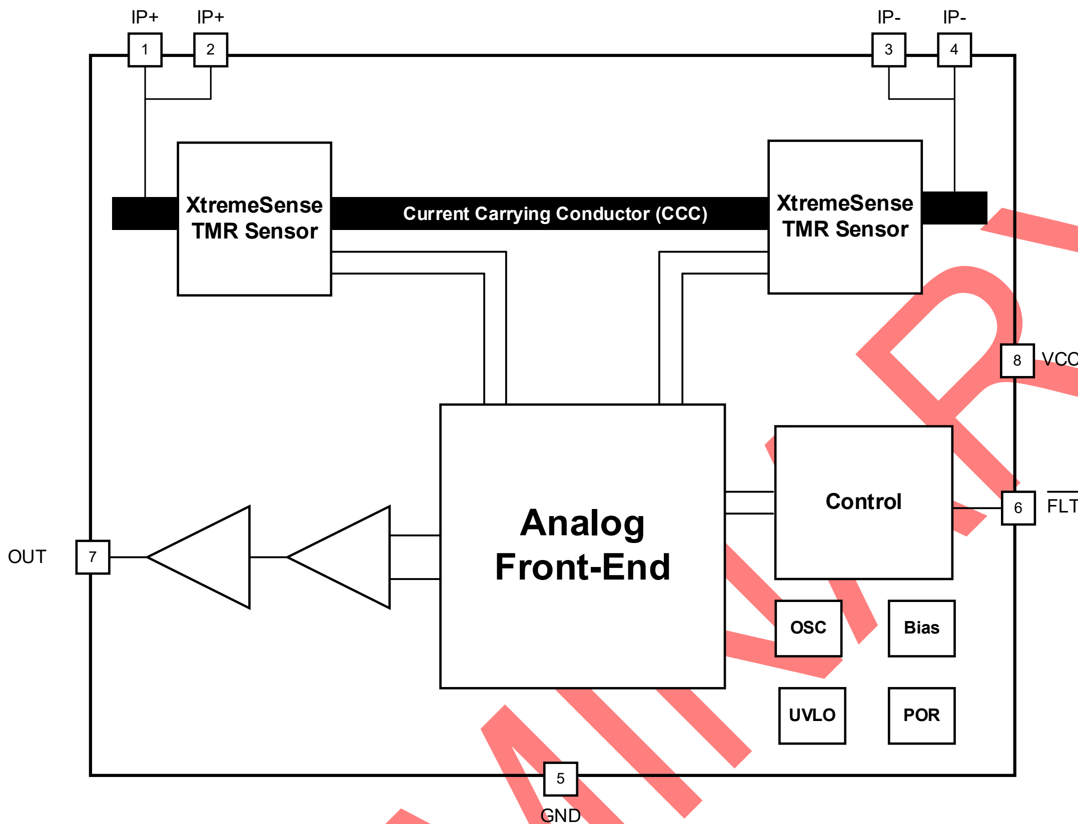


Figure 1. CT427 Functional Block Diagram for 8-lead SOIC Package

Application Diagram

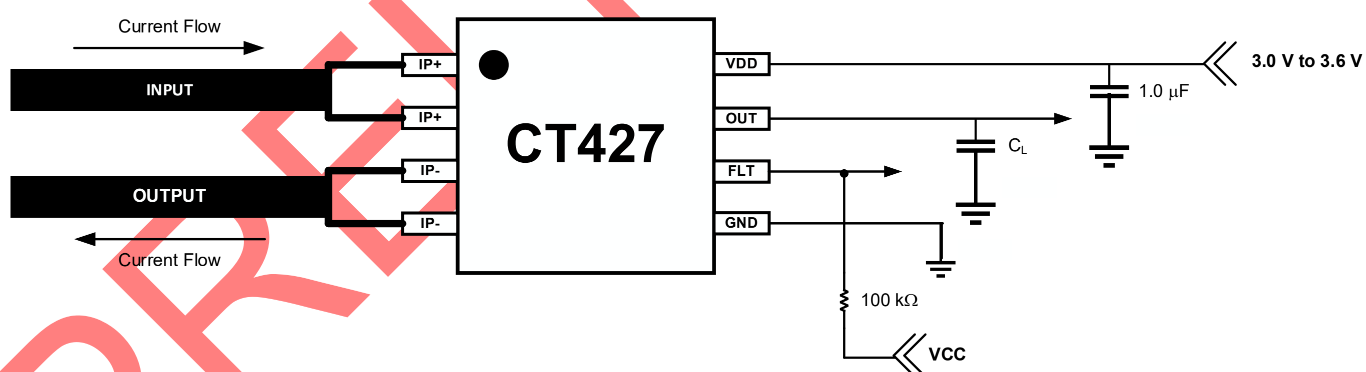


Figure 2. CT427 Application Block Diagram

Table 1. Recommended External Components

Component	Description	Vendor & Part Number	Parameter	Min.	Typ.	Max.	Unit
C_{BYP}	1.0 µF, X5R or Better	Murata GRM155C81A105KA12	C		1.0		µF

CT427 Pin Configuration

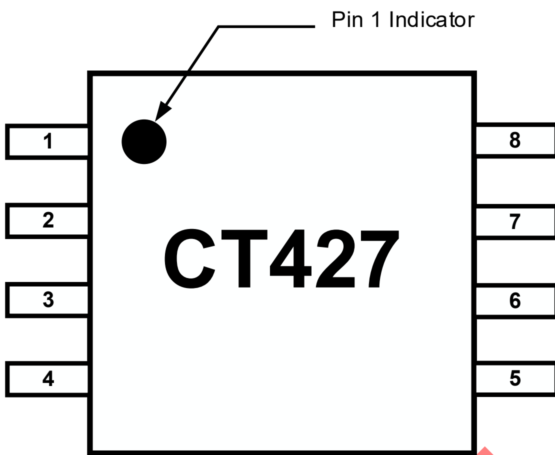


Figure 3. CT427 Pin-out Diagram for 8-lead SOIC Package (Top-Down View)

Pin Definition

Pin #	Pin Name	Pin Description
1	IP+	Input primary conductor (positive).
2		
3	IP-	Output primary conductor (negative).
4		
5	GND	Ground.
6	$\overline{\text{FLT}}$	Active LOW output fault signal (open drain output) to indicate that the following parameters are outside of normal operational bounds: • Over-Current Detection • UVLO If not used, then do not connect or connect to ground.
7	OUT	Analog output voltage that represents the measured current.
8	VDD	Supply voltage.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the CT427 and may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.3	6.0	V
$V_{I/O}$	Analog Input/Output Pins Maximum Voltage		-0.3	V_{CC} + 0.3*	V
$I_{CCC(MAX)}$	Current Carrying Conductor, T_A = +25°C			50	A
ESD	Electrostatic Discharge Protection Level	Human Body Model (HBM) per JESD22-A114	±2.0		kV
		Charged Device Model (CDM) per JESD22-C101	±0.5		
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+155	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

*The lower of V_{CC} + 0.3 V or 6.0 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual operation of the CT427. Recommended operating conditions are specified to ensure optimal performance to the specifications. Crocus Technology does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range		3.0	3.3	3.6	V
V_{OUT}	OUT Voltage Range		0		V_{CC}	V
I_{OUT}	OUT Current				±1.0	mA
T_A	Operating Ambient Temperature	Industrial	-40	+25	+85	°C
		Extended Industrial	-40	+25	+125	

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout and is determined in accordance to JEDEC standard JESD51 for a four (4) layer 2s2p FR-4 printed circuit board (PCB) with 2 oz. of copper (Cu). Special attention must be paid not to exceed junction temperature $T_{J(MAX)}$ at a given ambient temperature T_A.

Symbol	Parameter	Min.	Typ.	Max.	Unit
θ_{JA_SOIC}	Junction-to-Ambient Thermal Resistance, SOIC-8		151	176	°C/W
θ_{JC_SOIC}	Junction-to-Case Thermal Resistance, SOIC-8		102	128	°C/W

Isolation Specifications

Symbol	Parameter	Conditions	Rating	Unit
V_{ISO}	Rated Isolation Voltage	Agency Tested per IEC 62368* for 60 seconds. Production Tested at V_{ISO} for 1 second per IEC 62368.	3.0	kV_{RMS}
		Agency Tested per UL1577 for 60 seconds. Production Tested at V_{ISO} for 1 second per UL1577.	3.0	kV_{RMS}
V_{WORK_ISO}	Working Voltage for Basic Isolation	Tested per per IEC 62368*	991	V_{PK}
			701	V_{RMS}
V_{WORK_RI}	Working Voltage for Reinforced Isolation	Tested per IEC 62368*	487	V_{PK}
			344	V_{RMS}
d_{CR}	Creepage Distance	Minimum Distance Along Package Body from IP Pins to I/O Pins	4.96	mm
d_{CL}	Clearance Distance	Minimum Distance Through Air from IP Pins to I/O Pins	4.63	mm
d_{ISO}	Distance Through Isolation	Minimum Internal Distance Through Isolation	40	µm
CTI	Comparative Tracking Index	Material Group II	400 to 599	V

*IEC 62368 is the succeeding standard to IEC 60950-1 (Edition 2) for isolation testing specifications and as such it will be compliant to the latter standard.

Electrical Specifications

General Parameters

Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 µF. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_{CC}	Supply Current	f_{BW} = 1 MHz No load, I_P = 0 A		6.0	9.0	mA
I_{OUT}	OUT Maximum Drive Capability (1)	OUT covers 10% to 90% of V_{CC} span.	-1.0		+1.0	mA
C_{L_OUT}	OUT Capacitive Load (1)				100	pF
R_{L_OUT}	OUT Resistive Load (1)			100		kΩ
R_{IP}	Primary Conductor Resistance (1)			0.5		mΩ
Analog Output (OUT)						
V_{OUT}	OUT Voltage Linear Range	V_{SIG_AC} = ±1.00 V V_{SIG_DC} = +2.00 V	0.65		2.65	V
V_{OUT_SAT}	Output High Saturation Voltage	V_{OUT}, T_A = +25°C,	V_{CC} - 0.30	V_{CC} - 0.25		V
CMFR	Common Mode Field Rejection (1)			5.0		mA/mT

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TCS	Temperature Coefficient of Sensitivity	Absolute Value T_A = -40°C to +125°C		10	40	ppm/°C
TCO	Temperature Coefficient of Offset (1)	Absolute Value T_A = -40°C to +125°C		0.16		% FS
Fault Output ($\overline{FLT}$)						
$V_{FLT\#\_OL}$	$\overline{FLT}$ Voltage LOW	$I_{FLT\#\_OUT} \leq$ 20 mA	0		0.5	V
$I_{LEAK\_FLT\#}$	High Impedance Output Leakage Current	$V_{FLT\#\_OH} = V_{CC}$		5		µA
RPU	$\overline{FLT}$ Pull-up Resistor			100		kΩ
Timings						
t_{ON}	Power-On Time (1)	$V_{CC} \geq$ 2.50 V		100	200	µs
t_{RISE}	Rise Time (1)	$I_P = I_{RANGE(MAX)}$, T_A = +25°C, C_L = 220 pF		0.20		µs
$t_{RESPONSE}$	Response Time (1)			0.30		µs
t_{DELAY}	Propagation Delay (1)			0.25		µs
Protection						
V_{UVLO}	Under-Voltage Lockout	Rising V_{CC}		2.50		V
		Falling V_{CC}		2.45		V
V_{UV_HYS}	UVLO Hysteresis			50		mV

(1) Guaranteed by design and characterization; not tested in production.

CT427-xSN820MR: -20 A to +20 A

Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 µF. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{RANGE}	Current Range		-20		+20	A
V_{OQ}	Voltage Output Quiescent	T_A = +25°C, I_P = 0 A	1.645	1.650	1.655	V
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		50		mV/A
E_{OUT}	Total Output Error	$I_P = I_{P(MAX)}$		±1.0		% FS
E_{LIN}	Non-Linearity Error	I_P = -20 A to +20 A		±0.3		% FS
f_{BW}	Bandwidth (1)	Small Signal = -3 dB		1.0		MHz
e_N	Noise (1)	T_A = +25°C, f_{BW} = 100 kHz		11		mA_{RMS}
Lifetime Drift						
E_{TOT_DRIFT}	Total Output Error Lifetime Drift (1)	$I_P = I_{P(MAX)}$		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

CT427-xSN830MR: -30 A to +30 A

Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 µF. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{RANGE}	Current Range		-30		+30	A
V_{OQ}	Voltage Output Quiescent	T_A = +25°C, I_P = 0 A	1.645	1.650	1.655	V
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		33.3		mV/A
E_{OUT}	Total Output Error	$I_P = I_{P(MAX)}$		±1.0		% FS
E_{LIN}	Non-Linearity Error	I_P = -30 A to +30 A		±0.3		% FS
f_{BW}	Bandwidth (1)	Small Signal = -3 dB		1.0		MHz
e_N	Noise (1)	T_A = +25°C, f_{BW} = 100 kHz		12		mA_{RMS}
Lifetime Drift						
E_{TOT_DRIFT}	Total Output Error Lifetime Drift (1)	$I_P = I_{P(MAX)}$		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Circuit Description

Overview

The CT427 is a very high accuracy contact current sensor with an integrated current carrying conductor (CCC) that handles up to 30 A. It has very high sensitivity and a wide dynamic range with excellent accuracy (very low total output error) across temperature. This current sensor supports two (2) current ranges:

- -20 A to +20 A
- -30 A to +30 A

When current is flowing through the CCC, the XtemeSense TMR sensors inside the chip senses the field which in turn generates a differential voltage signals that then goes through the Analog Front-End (AFE) to output a current measurement with less than ±1.0% full-scale (FS) total output error (E_{OUT}).

The chip is designed to enable a very fast response time of 0.30 μs for the current measurement from the OUT pin as the bandwidth for the CT427 is 1.0 MHz. Even with a high bandwidth, the chip consumes a minimal amount of power.

Linear Output Current Measurement

The CT427 provides a continuous linear analog output voltage which represents the current measurement. The output voltage range of OUT is from 0.65 V to 2.65 V with a V_{OQ} of 0.65 V and 1.65 V for unidirectional and bidirectional currents, respectively. Figure 4 illustrates the output voltage range of the OUT pin as a function of the measured current.

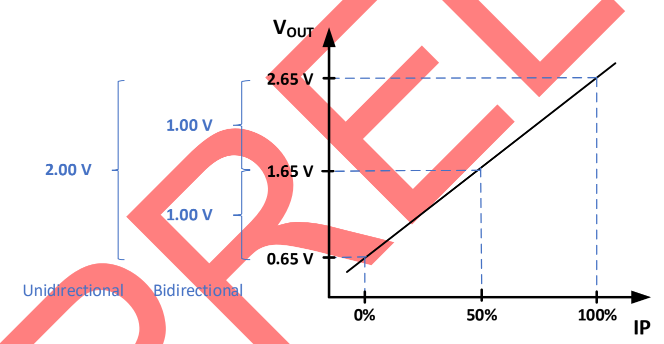


Figure 4. Linear Output Voltage Range (OUT) vs. Measured Current (IP)

Sensitivity

The Sensitivity (S) is a change in CT427's output in response to a change in 1 A of current flowing through the CCC. It is defined by the product of the magnetic circuit sensitivity (G/A, where 1.0 G = 0.1 mT) and the chip's linear amplifier gain (mV/G). Therefore, the result of this gives a sensitivity unit of mV/A. The CT427 is factory calibrated to optimize the sensitivity for the full scale of the device's dynamic range.

Total Output Error

The Total Output Error is the difference between the current measured by CT427 and the actual current, relative to the actual current. It is equivalent to the ratio between the difference of the ideal and actual voltage to the ideal sensitivity multiplied by the current flowing through the primary conductor (CCC). The following equation defines the Total Output Error (E_{OUT}) for the CT427:

$$E_{OUT} = \frac{V_{IOUT\_IDEAL}(I_P) - V_{IOUT}(I_P)}{S_{IDEAL}(I_P) \times I_P}$$

The E_{OUT} incorporates all sources of error and is a function of the sensed current (I_P) from CT427. At high current levels, the E_{OUT} will be dominated by the sensitivity error whereas at low current, the dominant characteristic is the offset voltage. Figure 5 shows the behavior of E_{OUT} versus I_P. When I_P goes to 0 from both directions, the curves exhibit asymptotic behavior i.e. E_{OUT} approaches infinity.

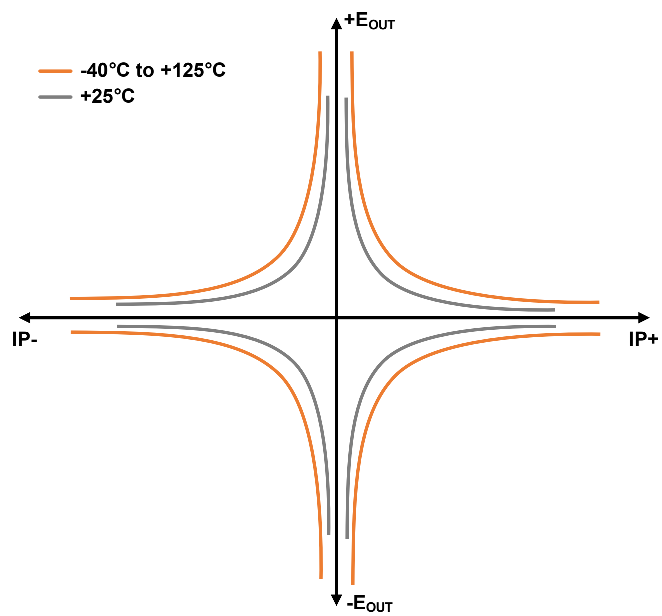


Figure 5. Total Output Error (E_{OUT}) vs. Sensed Current (IP)

The CT427 achieves a total output error (E_{OUT}) that is less than ±1.0% of Full-Scale (FS) over supply voltage and temperature. It is designed with innovative and proprietary TMR sensors and circuit blocks to provide very accurate current measurements regardless of the operating conditions.

Power-On Time (t_{ON})

The Power-On Time (t_{ON}) of 100 µs is the amount of time required by CT427 to start up, fully power the chip and becoming fully operational from the moment the supply voltage is applied to it. This time includes the ramp up time and the settling time (within 10% of steady-state voltage under an applied magnetic field) after the power supply has reached the minimum V_{CC}.

Response Time ($t_{RESPONSE}$)

The Response Time ($t_{RESPONSE}$) of 0.30 µs for the CT427 is the time interval between the following terms:

1. When the primary current signal reaches 90% of its final value,
2. When the chip reaches 90% of its output corresponding to the applied current.

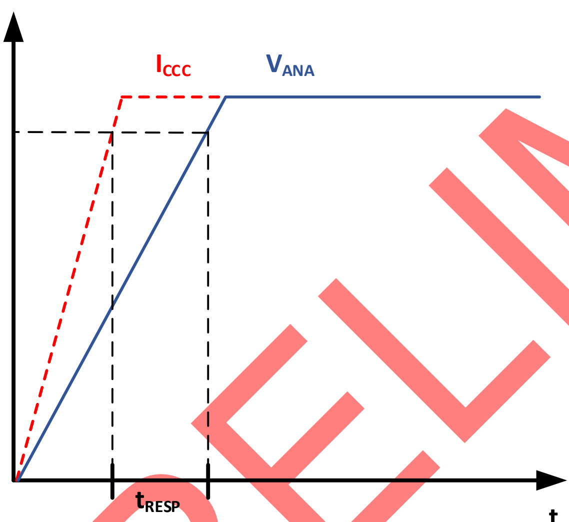


Figure 6. CT427 Response Time Curve

Rise Time (t_{RISE})

The CT427's rise time, t_{RISE}, is the time interval of when it reaches 10% and 90% of the full-scale output voltage. The t_{RISE} of the CT427 is 0.20 µs.

Propagation Delay (t_{DELAY})

The Propagation Delay (t_{DELAY}) is the time difference between these two events:

1. When the primary current reaches 20% of its final value
2. When the chip reaches 20% of its output corresponding to the applied current.

The CT427 has a propagation delay of 0.25 µs.

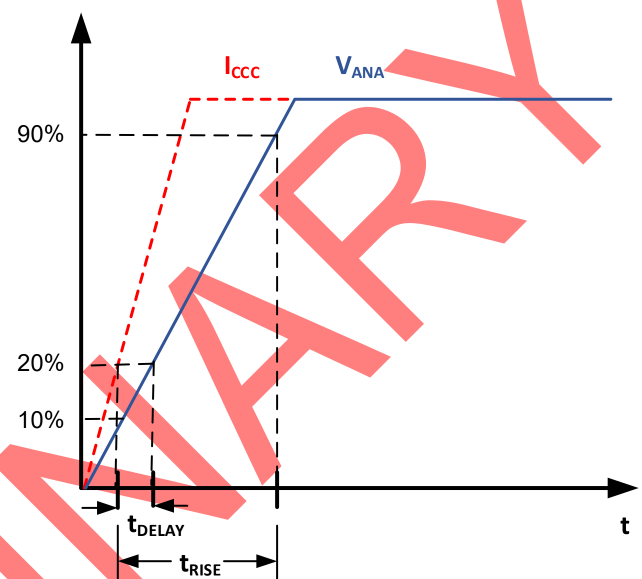


Figure 7. CT427 Propagation Delay and Rise Time Curve

Under-Voltage Lockout (UVLO)

The Under-Voltage Lock-out protection circuitry of the CT427 is activated when the supply voltage (V_{CC}) falls below 2.45 V. The CT427 remains in a low quiescent state until V_{CC} rises above the UVLO threshold (2.50 V). In this condition where the V_{CC} is less than 2.45 V and UVLO is triggered, the output from the CT427 is not valid and the $\overline{FLT}$ pin will go LOW. Once the V_{CC} rises above 2.50 V then the UVLO is cleared, and the $\overline{FLT}$ pin will be HIGH.

Fault# Interrupt ($\overline{FLT}$)

The CT427 generates an active LOW digital fault signal via the $\overline{FLT}$ pin to interrupt the microcontroller to indicate a fault event has been triggered. It is an open drain output and requires a pull-up resistor with a value of 100 kΩ tied to V_{CC}. A fault signal will interrupt the host system for these events:

- OCD
- UVLO

The $\overline{FLT}$ signal will be asserted LOW whenever one of the above fault events occur. In the case of an UVLO event, the $\overline{FLT}$ pin will stay LOW until the fault is cleared and then go HIGH.

If the $\overline{FLT}$ is not used, then it should be left unconnected or it can be connected to ground.

Immunity to Common Mode Fields

The CT427 is housed in custom plastic packages that utilize a "U-shaped" lead-frame to reduce the common mode fields generated as current flows through the CCC. With the "U-shaped" lead-frame, the stray fields cancel one another thus reducing electro-magnetic interference (EMI).

Also, good PCB layout of the CT427 will optimize performance and reduce EMI. Please see the Applications Information section in this data sheet for recommendations on PCB layout.

Creepage and Clearance

Two important terms as it relates to isolation provided by the package are: creepage and clearance. Creepage is defined as the shortest distance across the surface of the package from one side the leads to the other side of the leads. The definition for clearance is the shortest distance between the leads of opposite side through the air. Figure 8 illustrates the creepage and clearance for the SOIC-8 package of the CT427.

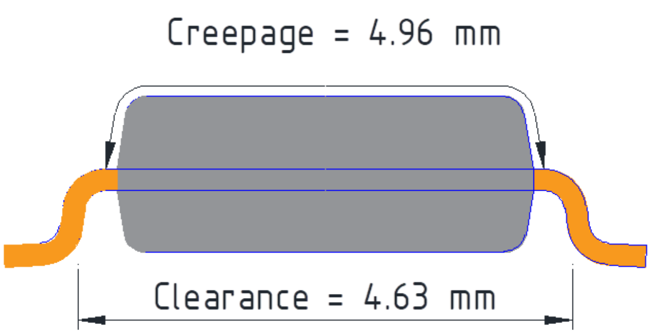


Figure 8. The Creepage and Clearance for the CT427's SOIC-8 package

Applications Information

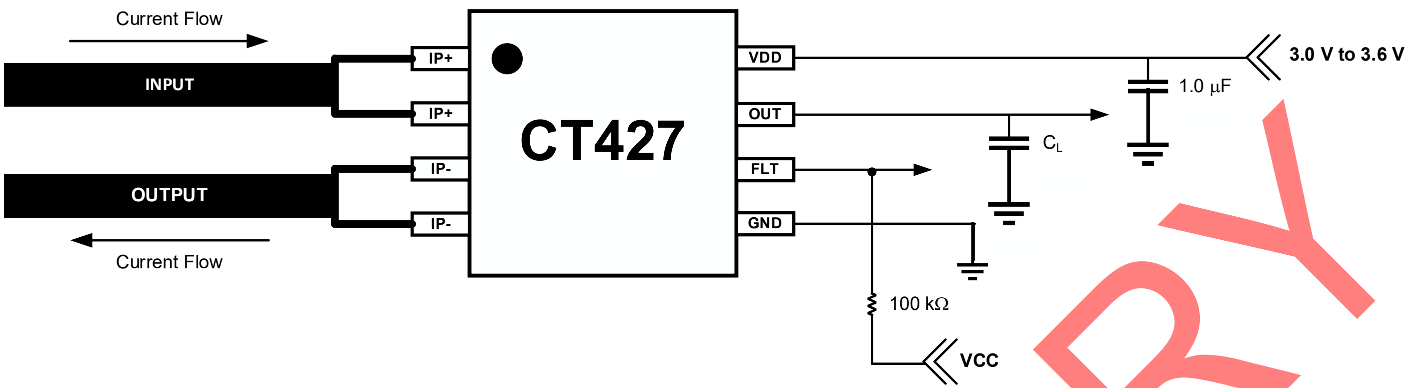


Figure 9. CT427 Application Block Diagram

Application

The CT427 is an integrated contact current sensor that can be used in many applications from measuring current in power supplies to motor control to over-current fault protection. It is a plug-and-play solution in that no calibration is required and it outputs to a microcontroller a simple linear analog output voltage which corresponds to a current measurement value.

It is designed to support an operating voltage range of 3.3 V to 3.6 V, but it is ideal to use a 3.3 V power supply where the output tolerance is less than ±5%.

Bypass Capacitor

A single 1.0 µF capacitor is needed for the VCC pin to reduce the noise from the power supply and other circuits. This capacitor should be placed as close as possible to the CT427 to minimize inductance and resistance between the two devices.

$\overline{\text{FLT}}$ Resistor

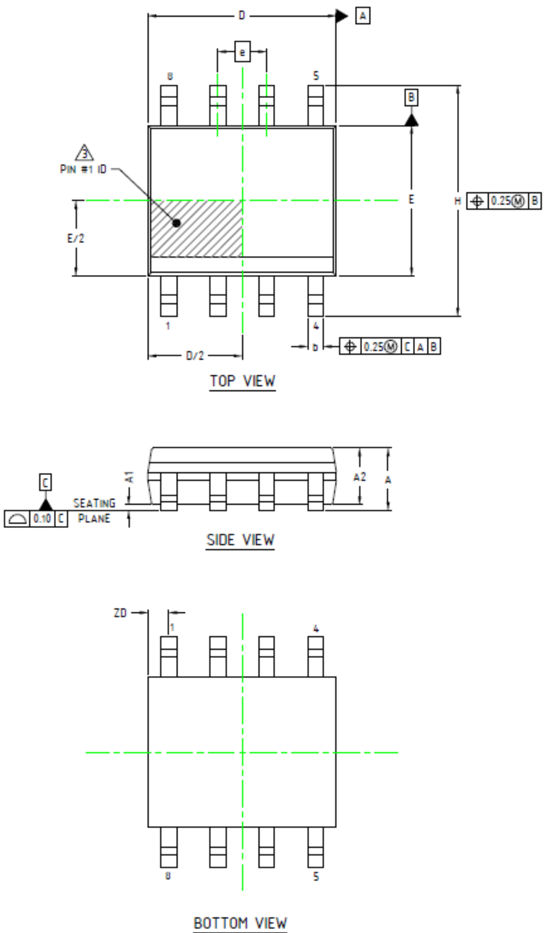
For the CT427, the FLT# pin is an open drain output. It requires a pull-up resistor value of 100 kΩ to be connected from the pin to V_{CC}.

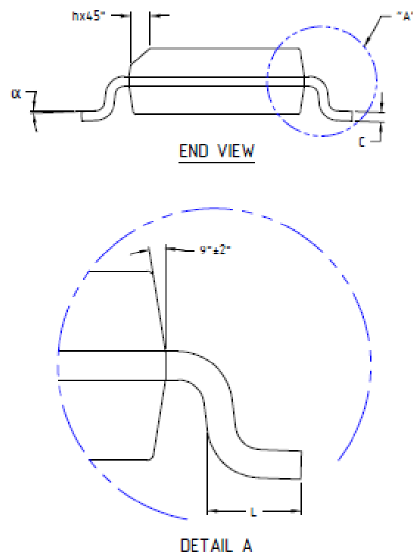
If the FLT# pin is not needed in the application, then this pin should not be connected and be left floating.

Recommended PCB Layout

Since the CT427 can measure up to 30 A of current, special care must be taken in the printed circuit board (PCB) layout of the CT427 and the surrounding circuitry. It is recommended that the CCC pins be connected to as much copper area as possible. It is also recommended that 2 oz. or heavier copper be used for PCB traces when the CT427 is used to measure 30 A of current. Additional layers of the PCB should also be used to carry current and be connected using the arrangement of vias.

SOIC-8 Package Drawing and Dimensions





NOTES

1. ALL DIMENSIONS IN MM.
2. PACKAGE SURFACE FINISHING:
   2.1. TOP : MATTE (CHARMILLES #18~30)
   2.2. BOTTOM : MATTE (CHARMILLES #12~27)
3. THE PIN #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED.
4. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM MAX.
5. JEDEC REFERENCE : MS-012.

Figure 10. SOIC-8 Package Drawing

Table 2. CT427 SOIC-8 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A1	0.10	0.18	0.25
b	0.36	0.41	0.46
C	0.19	0.22	0.25
D	4.80	4.89	4.98
E	3.81	3.90	3.99
e		1.27 BSC	
H	5.80	6.00	6.20
h	0.25	0.37	0.50
L	0.41	-	1.27
A	1.52	1.62	1.72
α	0°	-	8°
ZD		0.53 REF	
A2	1.37	1.47	1.57

Crocus Technology provides package drawings as a service to customers considering or planning to use Crocus products in their designs. Drawings may change without notice. Please note the revision and date of the data sheet and contact a Crocus Technology representative to verify or obtain the most recent version. The package specifications do not expand the terms of Crocus Technology's worldwide terms and conditions, specifically the warranty therein, which covers Crocus Technology's products.

Package Information

Table 3. CT427 Package Information

Part Number	Package Type	# of Leads	Package Quantity	Lead Finish	MSL Rating (2)	Operating Temperature (3)	Device Marking
CT427-ESN820MR	SOIC	8	100	Sn	3	-40°C to +85°C	CT427 S820MR
CT427-HSN820MR	SOIC	8	100	Sn	3	-40°C to +125°C	CT427 S820MR
CT427-ESN830MR	SOIC	8	100	Sn	3	-40°C to +85°C	CT427 S830MR
CT427-HSN830MR	SOIC	8	100	Sn	3	-40°C to +125°C	CT427 S830MR

(1) RoHS is defined as semiconductor products that are compliant to the current EU RoHS requirements. It also will meet the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Green is defined as the content of Chlorine (Cl), Bromine (Br) and Antimony Trioxide based flame retardants satisfy JS709B low halogen requirements of ≤ 1,000 ppm.

(2) MSL Rating = Moisture Sensitivity Level Rating as defined by JEDEC standard classifications.

(3) Package will withstand ambient temperature range of -40°C to +125°C and storage temperature range of -65°C to +150°C.

Device Marking

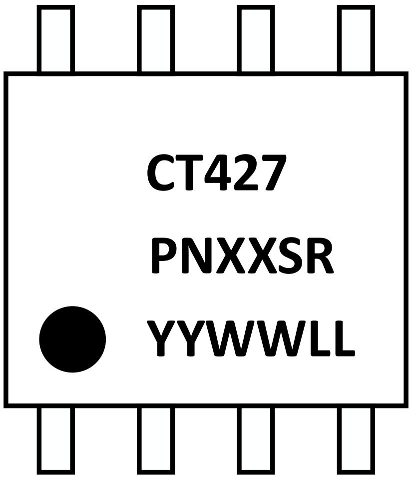


Figure 11. CT427 Device Marking for 8-lead Package

Row No.	Code	Definition
3	•	Pin 1 Indicator
1	CT427	Crocus Part Number
2	P	Package Type
2	N	Number of Pins
2	XX	Maximum Current Rating
2	SR	Current Range
3	YY	Calendar Year
3	WW	Work Week
3	LL	Lot Code

Table 4. CT427 Device Marking Definition for 8-lead SOIC Package

Part Ordering Number Legend

CT 4 2 7 - T PKG XY ZR

Polarity
DR = Unipolar or DC Current
MR = Bipolar or AC Current

Current Range
20 = 20 A
30 = 30 A

Package Type
SN8 = 8-lead SOIC Narrow

Temperature Range
E = -40°C to +85°C
H = -40°C to +125°C

Current Sensor Variant
7 = Pin #6 is FLT#; V_{CC} = 3.3 V

Current Sensor Type
2 = Contact Current Sensor

Product Family
4 = Current Sensor

CT = Crocus Technology

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Product Status Definition

Data Sheet Identification	Product Status	Definition
Objective	Proposed New Product Idea or In Development	Data sheet contains design target specifications and are subject to change without notice at any time.
Preliminary	First Production	Data sheet contains preliminary specifications obtained by measurements of early samples. Follow-on data will be published at a later date as more test data is acquired. Crocus reserves the right to make changes to the data sheet at any time.
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